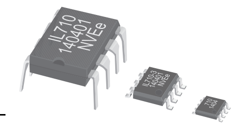
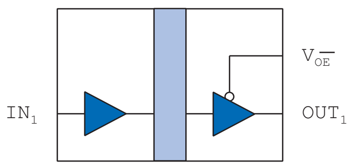
NVE CORPORATION

IL710

High Speed Single-Channel Digital Isolators



Functional Diagram



IL710

Truth Table

V_I	$V_{\overline{OE}}$	V_O
L	L	L
H	L	H
L	H	Z
H	H	Z

Features

- High Speed: 150 Mbps typical (IL710S)
- 2500 V_{RMS} isolation voltage
- 100 kV/µs common mode transient immunity
- No carrier or clock for low EMI emissions and susceptibility
- 2.7 to 5.5 volt supply range
- 1.2 mA/channel typical quiescent current
- 300 ps typical pulse width distortion (IL710S)
- 100 ps pulse jitter
- 2 ns channel-to-channel skew
- 10 ns typical propagation delay
- 44000 year barrier life
- Excellent magnetic immunity
- VDE V 0884 certified; UL 1577 recognized
- 500 V_{RMS} IS-to-IS intrinsically safe
- 8-pin MSOP, SOIC, and PDIP packages

Applications

- Digital Fieldbus
- RS-485 and RS-422
- Ground loop elimination
- Peripheral interfaces
- Serial communication
- Logic level shifting
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV_{RMS} rated IEC 60601-1 medical applications

Description

NVE's IL700 family of high-speed digital isolators are CMOS devices manufactured with NVE's patented* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion as low as 300 ps (0.3 ns), achieving the best specifications of any isolator. Minimum transient immunity of 100 kV/µs is unsurpassed. The IL710 is ideal for isolating applications such as PROFIBUS, RS-485, and RS-422.

The IL710 is available in 8-pin MSOP, SOIC, and PDIP packages.

The IL710S is the world's fastest isolator of its type, with a 150 Mbps typical data rate. Standard and S-Grade parts are specified over a temperature range of −40°C to +100°C. T-Grade parts are specified over a temperature range of −40°C to +125°C. The MSOP V-Series version offers full 2500 V_{RMS} isolation in an ultraminiature package.

IsoLoop is a registered trademark of NVE Corporation.
*U.S. Patent numbers 5,831,426; 6,300,617 and others.

REV. AH

Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	–55		150	°C	
Junction Temperature	T_J	–55		150	°C	
Ambient Operating Temperature(1) IL710T	T_A	–40		100 125	°C	
Supply Voltage	V_{DD1}, V_{DD2}	–0.5		7	V	
Input Voltage	V_I	–0.5		V_{DD1}+0.5	V	
Input Voltage	$V_{\overline{OE}}$	–0.5		V_{DD2}+0.5	V	
Output Voltage	V_O	–0.5		V_{DD2}+0.5	V	
Output Current Drive	I_O			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature IL710 and IL710S IL710T	T_A	 –40 –40		 100 125	 °C °C	
Junction Temperature IL710 and IL710S IL710T	T_J	 –40 –40		 110 125	 °C °C	
Supply Voltage	V_{DD1}, V_{DD2}	2.7		5.5	V	
Logic High Input Voltage	V_{IH}	2.4		V_{DD1}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	μs	

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Safety and Approvals

VDE V 0884-10 (VDE V 0884-11 pending)

Basic Isolation; VDE File Number 5016933-4880-0001

- Isolation voltage (V_{ISO}): 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}): 4000 V_{PK}
- Surge rating: 4000 V_{PK}
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit.
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit.

- Working Voltage (V_{IORM}; pollution degree 2):

Package	Part No. Suffix	Working Voltage
MSOP8	-1	399 V_{RMS}
PDIP8	-2	1000 V_{RMS}
SOIC8	-3	1000 V_{RMS}

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180 °C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

UL 1577 (Component Recognition Program File Number E207481)

- 2500 V rating for all types other than MSOP.
- Each part other than MSOP tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute.
- MSOP rating 1000 V; tested at 1200 V_{RMS} (1768 V_{PK}) for 1 second; each lot sample tested at 1500 V_{RMS} (2121 V_{PK}) for 1 minute.

ATEC / IEC 60079-0 / 60079-11 (Intrinsic Safety under Explosive Atmosphere Standards)

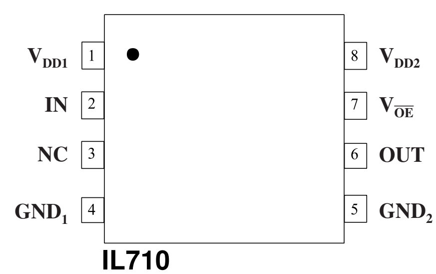
- IS-to-IS Certification pending
- 500 V_{RMS} rating

Soldering Profile

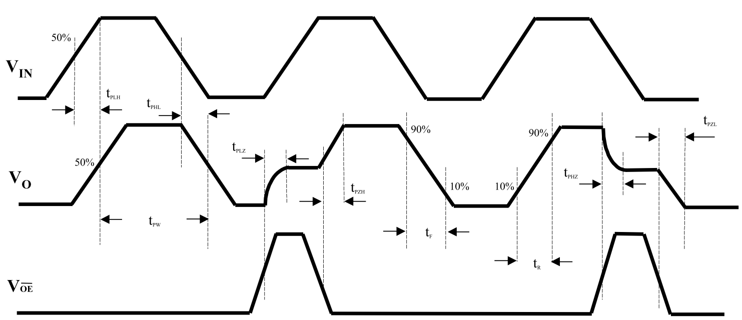
Per JEDEC J-STD-020C, MSL 1

IL710 Pin Connections

1	V_{DD1}	Supply voltage
2	IN	Data In
3	NC	No internal connection
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT	Data Out
7	$V_{\overline{OE}}$	Output enable. Internally held low with 100 kΩ
8	V_{DD2}	Supply voltage



Timing Diagram



Legend

t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_{PLZ}	Propagation Delay, Low to High Impedance
t_{PZH}	Propagation Delay, High Impedance to High
t_{PHZ}	Propagation Delay, High to High Impedance
t_{PZL}	Propagation Delay, High Impedance to Low
t_R	Rise Time
t_F	Fall Time

3.3 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current	I_{DD1}		8	10	µA	
Output Quiescent Supply Current	I_{DD2}		1.2	1.75	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD}−0.1	V_{DD}		V	I_O = −20 µA, $V_I = V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
			0.5	0.8		I_O = 4 mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 3.3 V)						
Maximum Data Rate						
IL710, IL710T, and IL710V		100	110		Mbps	C_L = 15 pF
IL710S		130	140		Mbps	C_L = 15 pF
Pulse Width[7]	PW	10	7.5		ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18	ns	C_L = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t_{PHZ}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t_{PLZ}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t_{PZH}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t_{PZL}		3	5	ns	C_L = 15 pF
Pulse Width Distortion[2]						
IL710, IL710T, and IL710V	PWD		2	3	ns	C_L = 15 pF
IL710S			1	3		
Pulse Jitter[10]	t_J		100		ps	C_L = 15 pF
Propagation Delay difference between any two parts[3]	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		2	4	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		2	4	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)[4]	$\|CM_H\|,\|CM_L\|$	100	150		kV/µs	Per IEC 60747
Dynamic Power Consumption[6]						
) Output side			140	240	µA/Mbps/ch	
Input side			20	40		

Magnetic Field Immunity[8] (V_{DD2} = 3 V, 3 V < V_{DD1} < 5.5 V)						
Power Frequency Magnetic Immunity	H_{PF}		1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		2000		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}		2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

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5 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current	I_{DD1}		10	15	µA	
Output Quiescent Supply Current	I_{DD2}		1.8	2.5	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD}−0.1	V_{DD}		V	I_O = −20 µA, $V_I = V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
			0.5	0.8		I_O = 4 mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 5 V)						
Maximum Data Rate IL710, IL710T, and IL710V IL710S		 100 130	 110 150		 Mbps Mbps	 C_L = 15 pF C_L = 15 pF
Pulse Width(7)	PW	10	7.5		ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		10	15	ns	C_L = 15 pF
Propagation Delay Enable to Output (High to High Impedance)	t_{PHZ}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (Low to High Impedance)	t_{PLZ}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to High)	t_{PZH}		3	5	ns	C_L = 15 pF
Propagation Delay Enable to Output (High Impedance to Low)	t_{PZL}		3	5	ns	C_L = 15 pF
Pulse Width Distortion(2) IL710, IL710T, and IL710V IL710S	PWD		 2 0.3	 3 3	ns	C_L = 15 pF
Propagation Delay difference between any two parts(3)	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)(4)	$\|CM_H\|,\|CM_L\|$	100	150		kV/µs	Per IEC 60747
Dynamic Power Consumption(6)						
) Output side			200	340	µA/Mbps/ch	
Input side			30	50		

Magnetic Field Immunity(8) (V_{DD2}= 5 V, 3 V < V_{DD1}< 5.5 V)						
Power Frequency Magnetic Immunity	H_{PF}		3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		4500		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}		4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

Insulation Specifications

Parameters		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)							
MSOP			3.01			mm	
SOIC			4.04			mm	
PDIP			6.8			mm	
Total Barrier Thickness (internal)			0.012	0.013		mm	
Leakage Current(5)				0.2		µA	240 V_{RMS}, 60 Hz
Barrier Resistance(5)		R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance(5)		C_{IO}		1.1		pF	f = 1 MHz
Comparative Tracking Index		CTI	≥175			V	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
	DC		1500			V_{DC}	
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	MSOP SOIC PDIP	θ_{JA}		184 134 114		°C/W	Double-sided PCB in free air
Junction–Case (Top) Thermal Resistance	MSOP SOIC PDIP	θ_{JC}		15 10 36		°C/W	
Power Dissipation	MSOP SOIC PDIP	P_D			500 675 800	mW	

Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
4. CM_H and CM_L are the maximum common mode voltage slew rates that can be applied with the outputs remaining stable and within V_{OL} and V_{OH} specifications.
5. Device is considered a two terminal device: pins 1–4 shorted and pins 5–8 shorted.
6. Dynamic power consumption is calculated per channel.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 7.
9. External magnetic field immunity is improved by this factor if the field direction is “end-to-end” rather than to “pin-to-pin” (see diagram on p. 7).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

Typical Performance Graphs

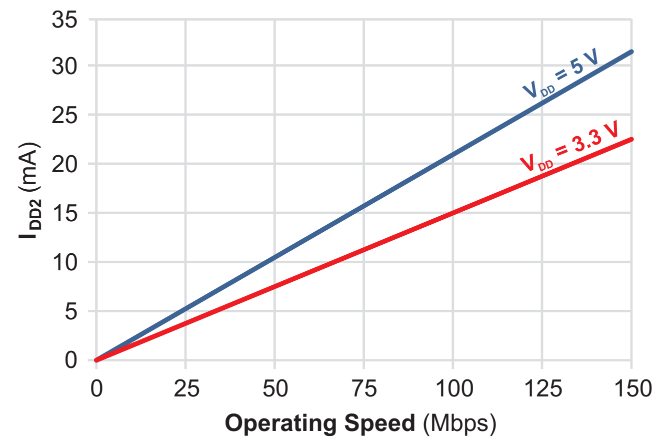


Figure 1. Supply current vs. operating speed.

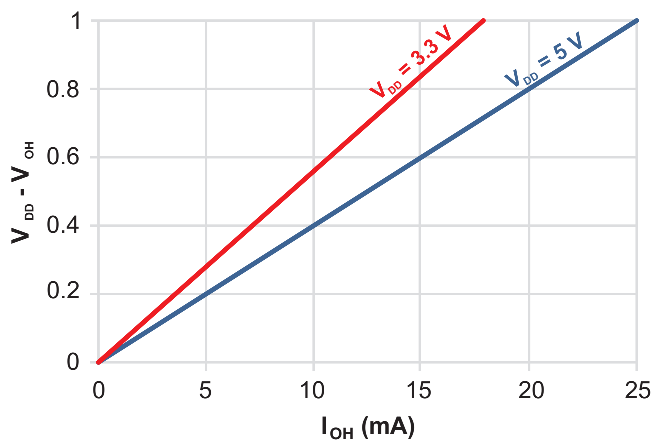


Figure 2. Typical high output voltage vs. load.

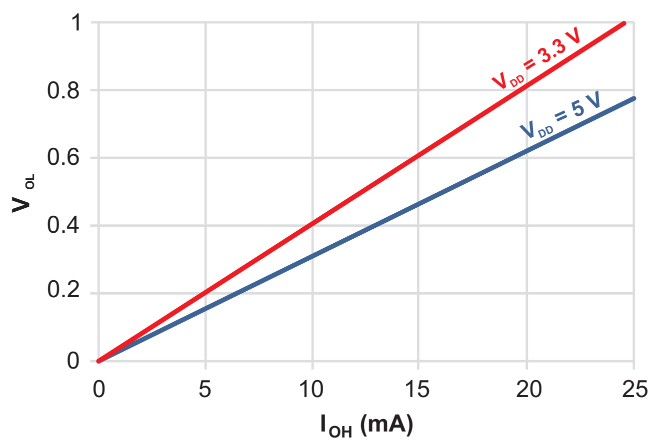
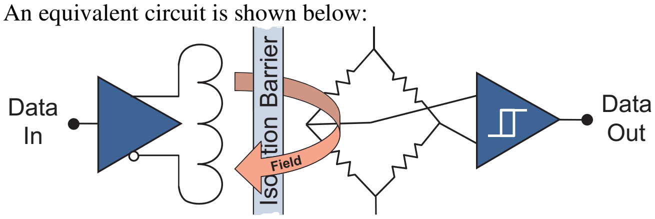


Figure 3. Typical low output voltage vs. load

Application Information

Isolator Operation

An equivalent circuit is shown below:



Isolator Signal Path

The GMR isolator signal path starts with a buffered input signal that is driven through an ultraminiature coil. This generates a small magnetic field that changes the electron spin polarization of GMR resistors, which are configured as a Wheatstone bridge. The change in spin polarization of the resistors creates a bridge voltage which drives an output comparator to construct an isolated version of the input signal.

Small Size, High Speed, and Low EMI

The coil, GMR, and circuitry are integrated to allow small packages. GMR is inherently high speed and low distortion, and unlike transformers, does not rely on energy transfer, so power is low and EMI emissions are minimal.

High Magnetic Immunity

GMR provides large signals which improve magnetic immunity, and the Wheatstone bridge configuration cancels ambient common-mode magnetic fields, further enhancing immunity to external magnetic fields.

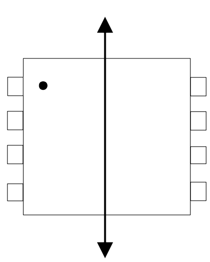
Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. These isolators are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



Cross-axis Field Direction

Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

Power Supply Decoupling

Both power supplies should be decoupled with 0.1 μF typical (0.047 μF minimum) capacitors as close as possible to the V_{DD} pins. Ground planes for both GND_1 and GND_2 are highly recommended for data rates above 10 Mbps.

Signal Status on Start-Up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

$$\text{PWD\%} = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \times 100\%$$

For example, with data rates of 12.5 Mbps:

$$\text{PWD\%} = \frac{3\text{ ns}}{80\text{ ns}} \times 100\% = 3.75\%$$

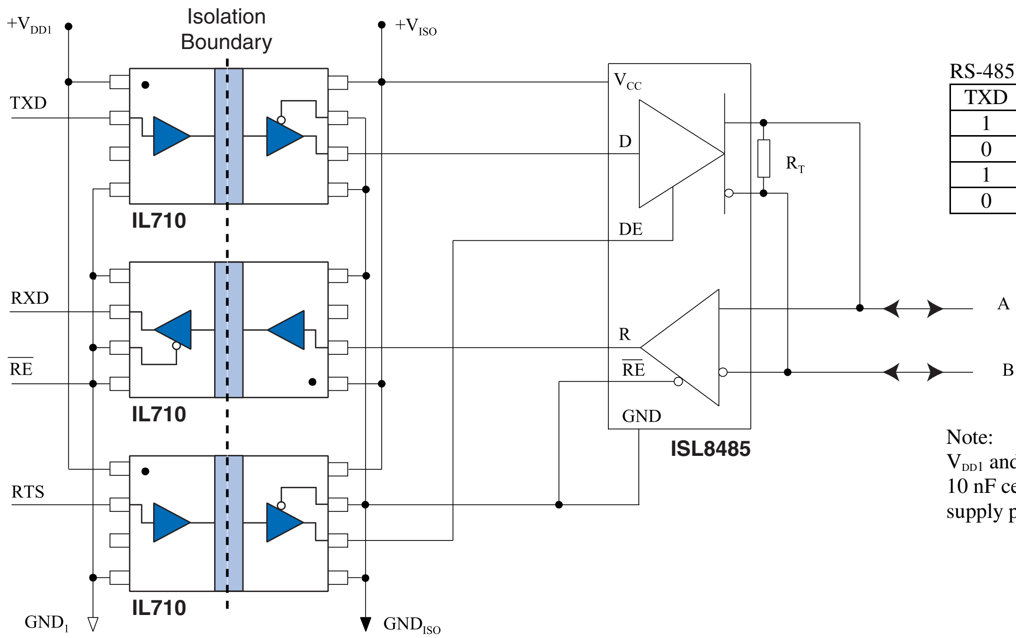
This figure is almost **three times** better than any available optocoupler with the same temperature range, and **two times** better than any optocoupler regardless of published temperature range. IsoLoop isolators exceed the 10% maximum PWD recommended by PROFIBUS, and will run to nearly 35 Mb within the 10% limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Short propagation delay skew is therefore especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in an IL700 Isolator is only 3 ns, which is **ten times** better than any optocoupler. IL700 Isolators have a maximum propagation delay skew of 6 ns, which is **five times** better than any optocoupler.

Application Diagrams

Isolated PROFIBUS / RS-485

NVE offers a unique line of single-chip isolated PROFIBUS/RS-485 transceivers, but as this circuit illustrates, IL710 isolators can also be used as part of multi-chip designs using non-isolated PROFIBUS transceivers:



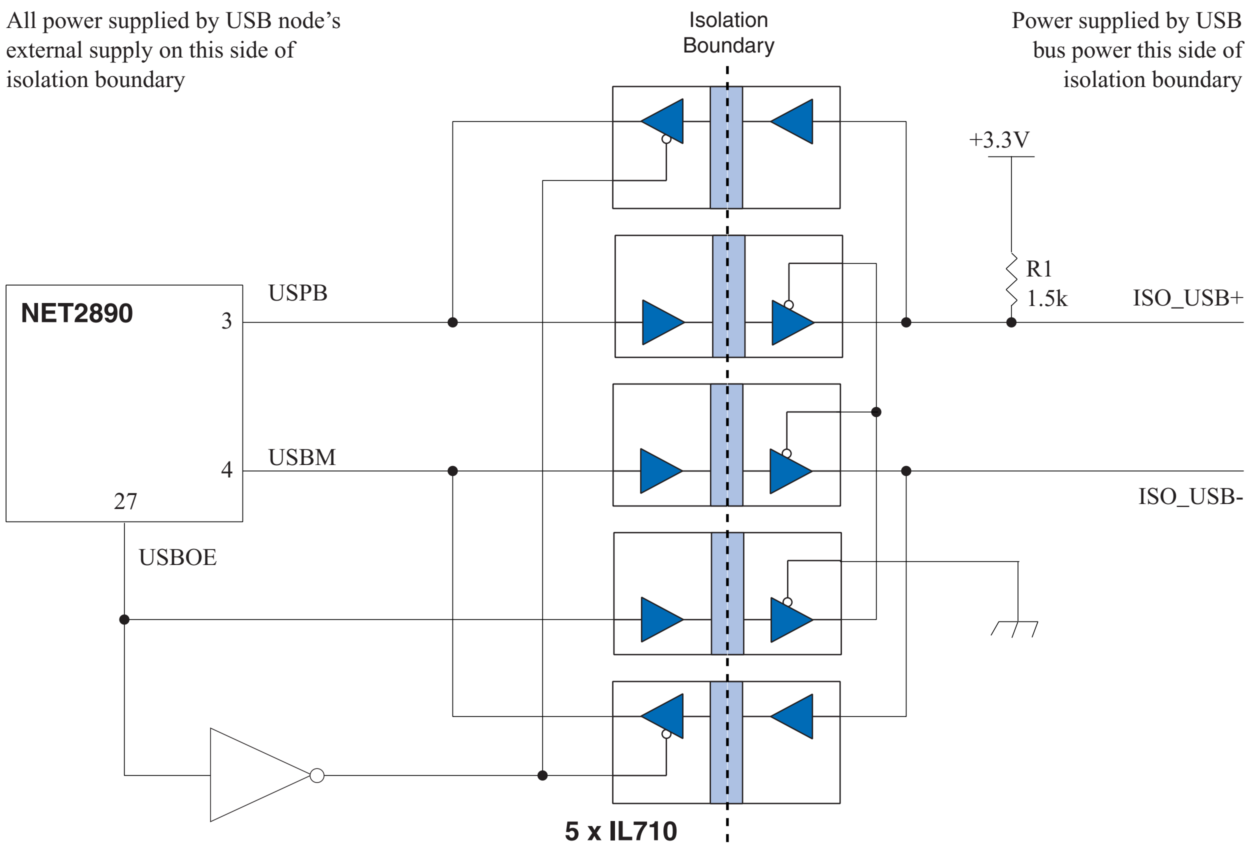
RS-485 Truth Table

TXD	RTS	A	B	RXD
1	0	Z	Z	X
0	0	Z	Z	X
1	1	1	0	1
0	1	0	1	0

Note:
V_{DD1} and V_{ISO} should be decoupled with 10 nF ceramic capacitors at IL710 supply pins.

Isolated USB

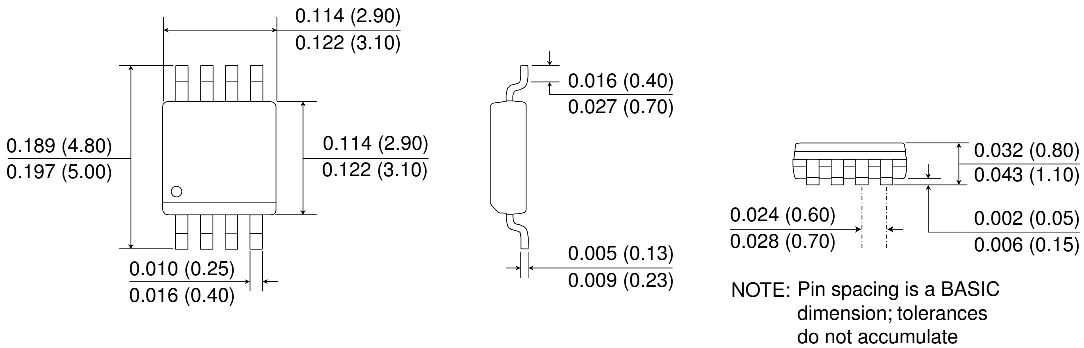
In this circuit, power is supplied by USB bus power on one side of the isolation barrier, and the USB node's external supply on the other side of the barrier. IL700 Isolators are specified with just 3 ns worst-case pulse width distortion:



Package Drawings

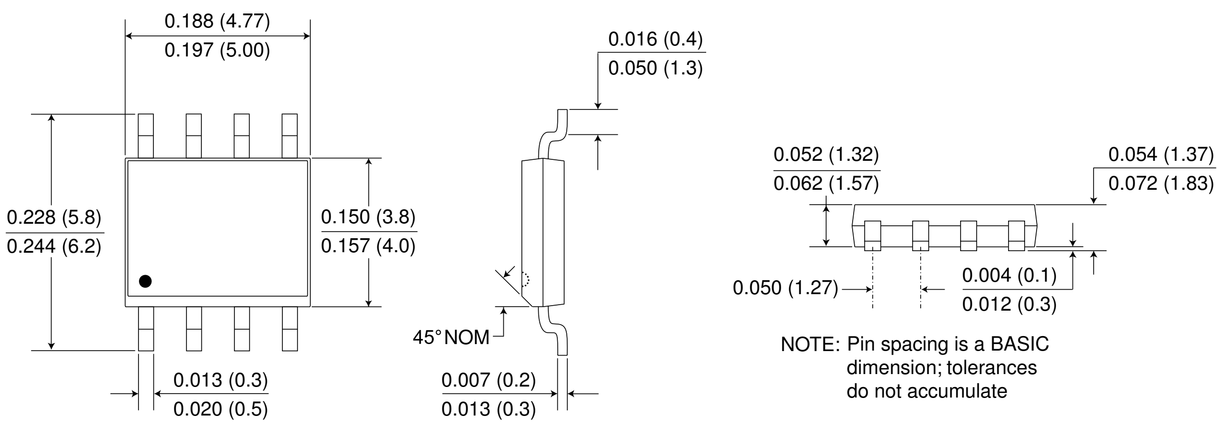
8-pin MSOP (-1 suffix)

Dimensions in inches (mm); scale = approx. 5X



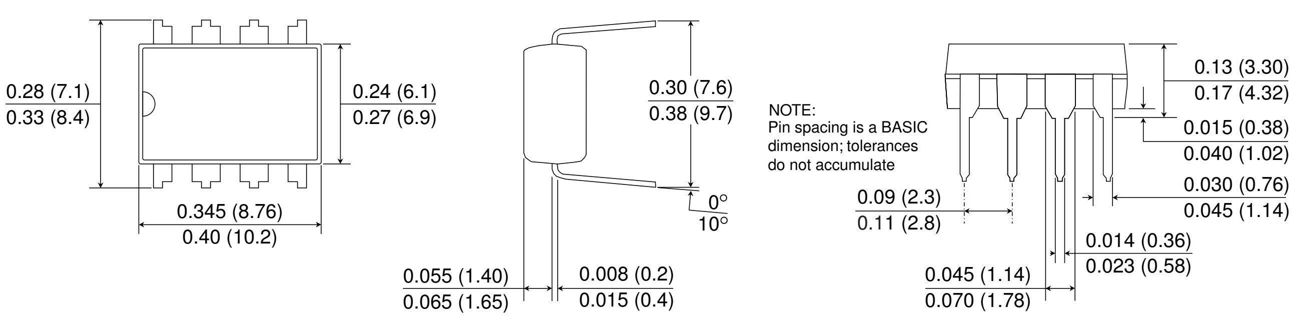
8-pin SOIC Package (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X



8-pin PDIP (-2 suffix)

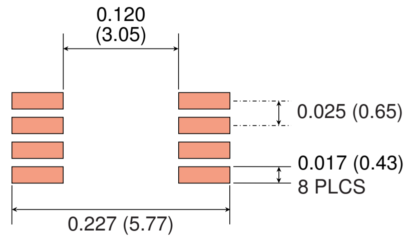
Dimensions in inches (mm); scale = approx. 2.5X



Recommended Pad Layouts

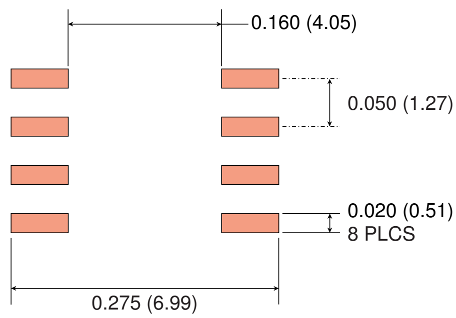
8-pin MSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X



8-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



Ordering Information and Valid Part Numbers

IL 710 T - 3 E TR13

Bulk Packaging
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

Package
Blank = 80/20 Tin/Lead Plating
E = RoHS Compliant

Package Type
-1 = MSOP
-2 = PDIP
-3 = 0.15" 8-pin SOIC

Grade
Blank = Standard
S = High Speed
T = High Temperature
V = High Isolation MSOP

Base Part Number
710 = Single Channel

Product Family
IL = Isolators

Valid Part Numbers

IL710-1E
IL710S-1E
IL710T-1E
IL710V-1E

IL710-2
IL710T-2
IL710-2E
IL710T-2E

IL710-3
IL710S-3
IL710T-3
IL710-3E
IL710S-3E
IL710T-3E

All MSOP and SOIC parts are available on tape and reel.

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ISB-DS-001-IL710-AH
November 2020

Changes

- Upgraded CMTI specifications.
- Added ATEC / IEC 60079 Intrinsic Safety pending (p. 3).
- Added output-side dynamic power consumption specifications (pp. 5 and 6).
- Changed "Propagation Delay Skew" to "Propagation Delay difference between any two parts" for clarity (pp. 5 and 6).

ISB-DS-001-IL710-AG

Changes

- Extended minimum operating power supplies to 2.7 volts.
- Updated EMC standards.
- Deleted minimum magnetic field immunity specifications since it is not 100% tested.
- Changed PDIP creepage specification from 7.04 mm to 6.8 mm (p. 6).
- Revised thermal properties (p. 6).
- Added Typical Performance Graphs (p. 7).
- More detailed description of operation (p. 8).

ISB-DS-001-IL710-AF

Change

- Updated SOIC8 package outline drawing.

ISB-DS-001-IL710-AE

Change

- Updated VDE approvals to VDE V 0884-10.

ISB-DS-001-IL710-AD

Change

- Added MSOP V-Series version (2500 VRMS isolation).

ISB-DS-001-IL710-AC

Changes

- Added product illustrations to first page.
- Revised and added details to thermal specifications (p. 2).
- Added VDE 0884 Safety-Limiting Values (p. 3).

ISB-DS-001-IL710-AB

Change

- IEC 60747-5-5 (VDE 0884) certification.

ISB-DS-001-IL710-AA

Changes

- Tighter quiescent current specifications.
- Upgraded from MSL 2 to MSL 1.

ISB-DS-001-IL710-Z

Changes

- Increased transient immunity specifications based on additional data.
- Added VDE 0884 pending.
- Added high voltage endurance specification.
- Increased magnetic immunity specifications.
- Updated package drawings.
- Added recommended solder pad layouts.

ISB-DS-001-IL710-Y

Changes

- Detailed isolation and barrier specifications.
- Cosmetic changes.

ISB-DS-001-IL710-X

Changes

- Tightened typ. output quiescent supply spec. from 1.7 mA to 1.5 mA.
- T-Series quiescent supply specs. tightened to be the same as other grades.

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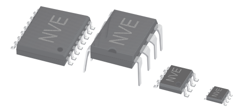
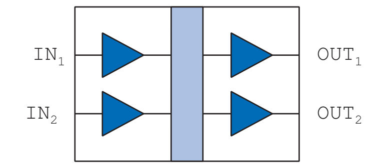
ISB-DS-001-IL710-AH

November 2020

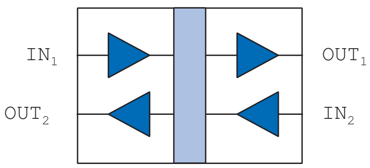
High Speed Two-Channel Digital Isolators



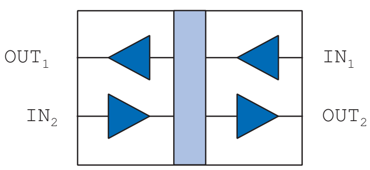
Functional Diagrams



IL711



IL712



IL721

Features

- High speed: 150 Mbps typical (S-Series)
- High temperature: −40 °C to +125 °C (T-Series and V-Series)
- Very high isolation: 6 kV_{RMS} Reinforced Isolation (V-Series)
- 2.7 to 5.5 volt supply range
- 100 kV/µs Common Mode Transient Immunity
- No carrier or clock for low EMI emissions and susceptibility
- 1.2 mA/channel typical quiescent current
- 300 ps typical pulse width distortion (S-Series)
- 100 ps pulse jitter
- 2 ns channel-to-channel skew
- 10 ns typical propagation delay
- 44000 year barrier life
- Excellent magnetic immunity
- VDE V 0884 certified; UL 1577 recognized
- 500 V_{RMS} IS-to-IS intrinsically safe
- MSOP, SOIC, PDIP, and True 8 mm creepage packages

Applications

- Board-to-board communication
- CANbus
- Peripheral interfaces
- Logic level shifting
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV_{RMS} rated IEC 60601-1 medical applications

Description

NVE's IL700 family of high-speed digital isolators are CMOS devices manufactured with NVE's patented* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology. A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

The IL711S and IL712S are the world's fastest two-channel isolators, with a 150 Mbps typical data rate for both channels. Standard and S-Grade parts are specified over a temperature range of −40°C to +100°C; "T" and "V" Grade parts have a maximum operating temperature of 125°C. V- Grade versions offer extremely high isolation voltages of 6 kV_{RMS} for wide-body packages and 2.5 kV_{RMS} for MSOPs.

The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion as low as 300 ps (0.3 ns), achieving the best specifications of any isolator. Minimum transient immunity of 100 kV/µs is unsurpassed.

The IL711 has two transmit channels; the IL712 and IL721 have one transmit and one receive channel. The IL721 has channels reversed to better suit certain board layouts.

The IL711 and IL712 are available in 8-pin MSOP, SOIC, and PDIP packages. The IL711 and IL721 are also available in NVE's unique JEDEC-compliant 16 pin package with True 8 mm creepage under IEC 60601.

IsoLoop is a registered trademark of NVE Corporation.
*U.S. Patent numbers 5,831,426; 6,300,617 and others.

Rev. AN

Absolute Maximum Ratings

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	–55		150	°C	
Junction Temperature	T_J	–55		150	°C	
Ambient Operating Temperature(1)	T_A	–55		130	°C	
Supply Voltage	V_{DD1}, V_{DD2}	–0.5		7	V	
Input Voltage	V_I	–0.5		V_{DD} + 0.5	V	
Output Voltage	V_O	–0.5		V_{DD} + 0.5	V	
Output Current Drive	I_O			10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature IL711/IL712/IL721/IL711S/IL712S IL711T/IL711VE/IL712T/IL721T/IL721VE	T_A	–40		100 125	°C °C	
Junction Temperature IL711/IL712/IL721/IL711S/IL712S IL711T/IL711VE/IL712T/IL721T/IL721VE	T_J	–40		110 125	°C °C	
Supply Voltage	V_{DD1}, V_{DD2}	2.7		5.5	V	
Logic High Input Voltage	V_{IH}	2.4		V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	μs	

Safety and Approvals

VDE V 0884-10 (VDE V 0884-11 pending)

VE versions (0.3" SOIC Reinforced Isolation; VDE File Number 5016933-4880-0002)

- Working Voltage (V_{IORM}) 1000 V_{RMS} (1415 V_{PK}); reinforced insulation; pollution degree 2
- Isolation voltage (V_{ISO}) 6000 V_{RMS}
- Surge immunity (V_{IOSM}) 12.8 kV_{PK}
- Surge rating 8 kV
- Transient overvoltage (V_{IOTM}) 6000 V_{PK}
- Each part tested at 2387 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 6000 V_{PK} for 60 sec.; then 2122 V_{PK} for 10 sec. with 5 pC partial discharge limit

Standard versions (Basic Isolation; VDE File Number 5016933-4880-0001)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Isolation voltage (V_{ISO}) 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}) 4000 V_{PK}
- Surge rating 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180°C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)

Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-1	MSOP (standard)	150 V_{RMS}
V-1	MSOP (high isolation voltage)	300 V_{RMS}
-2	PDIP	300 V_{RMS}
-3	SOIC	150 V_{RMS}
None	0.3" SOIC (standard)	300 V_{RMS}
VE	0.3" SOIC (high isolation voltage)	1000 V_{RMS}

UL 1577 (Component Recognition Program File Number E207481)

- 1 kV-rated standard MSOPs tested at 1200 V_{RMS} (1768 V_{PK}) for 1 second; each lot sample tested at 1200 V_{RMS} (1768 V_{PK}) for 1 minute
- 2.5 kV-rated parts tested at 3000 V_{RMS} (4240 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3530 V_{PK}) for 1 minute
- 6 kV-rated VE-version parts tested at 7.2 kV_{RMS} (10.2 kV_{PK}) for 1 second; each lot sample tested at 6 kV_{RMS} (8485 V_{PK}) for 1 minute

ATEC / IEC 60079-0 / 60079-11 (Intrinsic Safety under Explosive Atmosphere Standards)

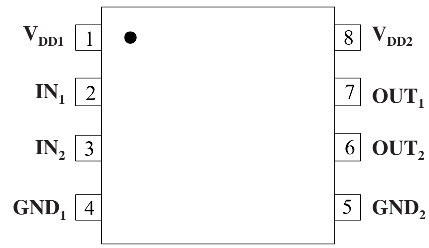
- IS-to-IS Certification pending
- 500 V_{RMS} rating

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

IL711-1, -2, and -3 Pin Connections

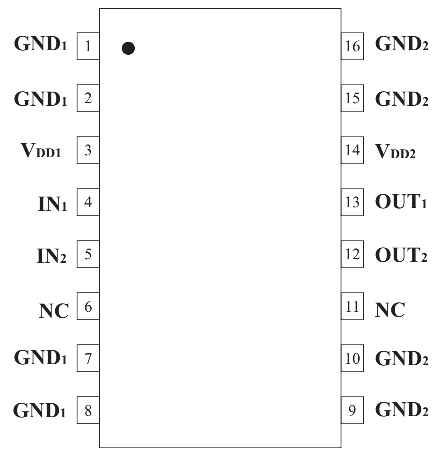
1	V_{DD1}	Supply voltage
2	IN_1	Data in, channel 1
3	IN_2	Data in, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT_2	Data out, channel 2
7	OUT_1	Data out, channel 1
8	V_{DD2}	Supply voltage



IL711-1, -2, and -3

IL711 Pin Connections

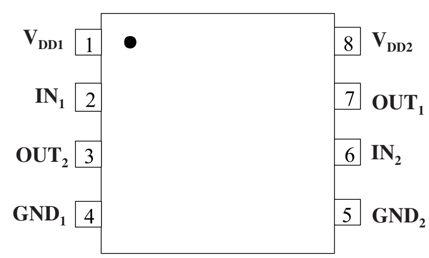
1 2	GND_1	Ground return for V_{DD1} (pins 1, 2, 7, and 8 internally connected)
3	V_{DD1}	Supply voltage
4	IN_1	Data in, channel 1
5	IN_2	Data in, channel 2
6	NC	No connection
7 8	GND_1	Ground return for V_{DD1} (pins 1, 2, 7, and 8 internally connected)
9 10	GND_2	Ground return for V_{DD2} (pins 9, 10, 15, and 16 internally connected)
11	NC	No connection
12	OUT_2	Data out, channel 2
13	OUT_1	Data out, channel 1
14	V_{DD2}	Supply voltage
15 16	GND_2	Ground return for V_{DD2} (pins 9, 10, 15, and 16 internally connected)



IL711

IL712-1, -2, and -3 Pin Connections

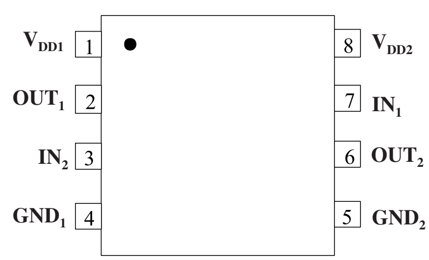
1	V_{DD1}	Supply voltage
2	IN_1	Data in, channel 1
3	OUT_2	Data out, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	IN_2	Data in, channel 2
7	OUT_1	Data out, channel 1
8	V_{DD2}	Supply voltage



IL712-1, -2, and -3

IL721-3 Pin Connections

1	V_{DD1}	Supply voltage
2	OUT_1	Data out, channel 1
3	IN_2	Data in, channel 2
4	GND_1	Ground return for V_{DD1}
5	GND_2	Ground return for V_{DD2}
6	OUT_2	Data out, channel 2
7	IN_1	Data in, channel 1
8	V_{DD2}	Supply voltage



IL721-3

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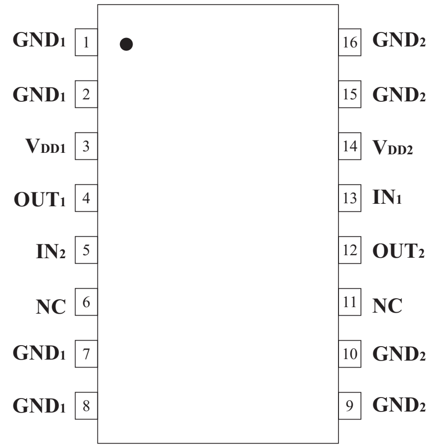
IL721 Pin Connections

1 2	GND_1	Ground return for V_{DD1} (pins 1, 2, 7, and 8 internally connected)
3	V_{DD1}	Supply voltage
4	OUT_1	Data out, channel 1
5	IN_2	Data in, channel 2
6	NC	No connection
7 8	GND_1	Ground return for V_{DD1} (pins 1, 2, 7, and 8 internally connected)
9 10	GND_2	Ground return for V_{DD2} (pins 9, 10, 15, and 16 internally connected)
11	NC	No connection
12	OUT_2	Data out, channel 2
13	IN_1	Data in, channel 1
14	V_{DD2}	Supply voltage
15 16	GND_2	Ground return for V_{DD2} (pins 9, 10, 15, and 16 internally connected)



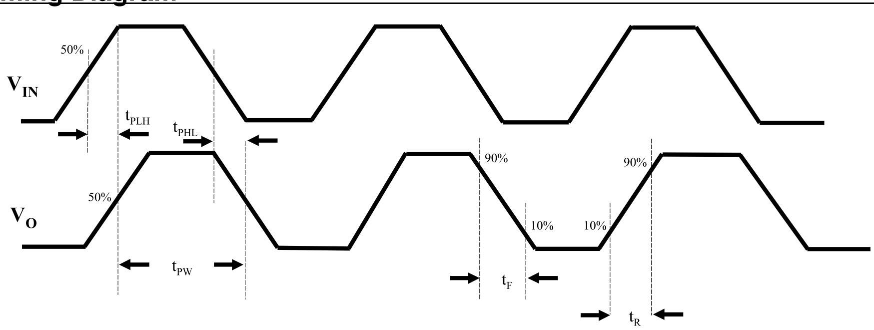
IL721

3.3 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current						
IL711	I_{DD1}		8	10	µA	
IL712/IL721			1.2	1.75	mA	
Output Quiescent Supply Current						
IL711	I_{DD2}		2.4	3.5	mA	
IL712/IL721			1.2	1.75	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} – 0.1	V_{DD}		V	I_O = −20 µA, $V_I = V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}			I_O = −4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, $V_I = V_{IL}$
			0.5	0.8		I_O = 4 mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 3.3 V)						
Maximum Data Rate IL711/IL712/IL721 IL711S/IL712S IL711T/IL712T/IL721T		 100 130 100	 110 140 110		 Mbps Mbps Mbps	 C_L = 15 pF C_L = 15 pF C_L = 15 pF
Pulse Width(7)	PW	10	7.5		ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18	ns	C_L = 15 pF
Pulse Width Distortion(2) IL711/IL712/IL721 IL711S/IL712S IL711T/IL712T/IL721T	PWD		 2 2 1	 3 3 3	 ns ns ns	 C_L = 15 pF C_L = 15 pF C_L = 15 pF
Propagation Delay difference between any two parts(3)	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		2	4	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		2	4	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)(4)	$\|CM_H\|,\|CM_L\|$	100	150		kV/µs	Per IEC 60747
Channel-to-Channel Skew	t_{CSK}		2	3	ns	C_L = 15 pF
Dynamic Power Consumption(6)						
Output side			140	240	µA/Mbps/ch	
Input side			20	40		

Magnetic Field Immunity(8) (V_{DD2} = 3.3 V, 2.7 V < V_{DD1} < 5.5 V)						
Power Frequency Magnetic Immunity	H_{PF}		1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		2000		A/m	t_p = 8 µs
Damped Oscillatory Magnetic Field	H_{OSC}		2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

Timing Diagram



Legend

t_{PLH}	Propagation Delay, Low to High
t_{PHL}	Propagation Delay, High to Low
t_{PW}	Minimum Pulse Width
t_R	Rise Time
t_F	Fall Time

5 Volt Electrical Specifications (T_{min} to T_{max} unless otherwise stated)						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Supply Current						
IL711	I_{DD1}		10	15	µA	
IL712/IL721			1.8	2.5	mA	
Output Quiescent Supply Current						
IL711	I_{DD2}		3.6	5	mA	
IL712/IL721			1.8	2.5	mA	
Logic Input Current	I_I	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD} − 0.1	V_{DD}		V	$I_O = -20$ µA, $V_I = V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}			$I_O = -4$ mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	$I_O = 20$ µA, $V_I = V_{IL}$
			0.5	0.8		$I_O = 4$ mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 5 V)						
Maximum Data Rate						
IL711/IL712/IL721		100	110		Mbps	C_L = 15 pF
IL711S/IL712S		130	150		Mbps	C_L = 15 pF
IL711T/IL712T/IL721T		100	110		Mbps	C_L = 15 pF
Pulse Width(7)	PW	10	7.5		ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		10	15	ns	C_L = 15 pF
Pulse Width Distortion(2)	PWD					
IL711/IL712/IL721			2	3	ns	C_L = 15 pF
IL711S/IL712S			2	3	ns	C_L = 15 pF
IL711T/IL712T/IL721T			0.3	3	ns	C_L = 15 pF
Pulse Jitter(10)	t_J		100		ps	C_L = 15 pF
Propagation Delay difference between any two parts(3)	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High or Logic Low)(4)	$\|CM_H\|,\|CM_L\|$	100	150		kV/µs	Per IEC 60747
Channel to Channel Skew	t_{CSK}		2	3	ns	C_L = 15 pF
Dynamic Power Consumption(6)						
Output side			200	340	µA/Mbps/ch	
Input side			30	50		

Magnetic Field Immunity(8) (V_{DD2}= 5 V, 2.7 V < V_{DD1} < 5.5 V)						
Power Frequency Magnetic Immunity	H_{PF}		3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		4500		A/m	t_p = 8 µs
Damped Oscillatory Magnetic Field	H_{OSC}		4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier(9)	K_X		2.5			

Insulation Specifications						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Creepage Distance (external)						
MSOP8		3.01			mm	
SOIC8		4.03			mm	
PDIP8		6.8			mm	
True 8™ 0.3" SOIC16		8.03	8.3		mm	Per IEC 60601
Total Barrier Thickness (internal)		0.012	0.016		mm	
Leakage Current(5)			0.2		µA	240 V_{RMS}, 60 Hz
Barrier Resistance(5)	R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance(5)	C_{IO}		2		pF	f = 1 MHz
Comparative Tracking Index	CTI	≥600			V_{RMS}	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life) DC	V_{IO}	1500			V_{DC}	At maximum operating temperature
Surge Immunity ("VE" Versions)	V_{IOSM}	12.8			kV_{PK}	Per IEC 61000-4-5
Barrier Life			44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics							
Parameter		**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Junction–Ambient Thermal Resistance	MSOP8 0.15" SOIC8 0.3" SOIC16 PDIP8	θ_{JA}		184 134 67 114		°C/W	Double-sided PCB in free air
Junction–Case (Top) Thermal Resistance	MSOP8 0.15" SOIC8 0.3" SOIC16 PDIP8	θ_{JC}		15 10 12 36		°C/W	Double-sided PCB in free air
Junction–Ambient Thermal Resistance	0.3" SOIC	θ_{JA}		46		°C/W	2s2p PCB in free air per JESD51
Junction–Case (Top) Thermal Resistance	0.3" SOIC	θ_{JC}		9		°C/W	2s2p PCB in free air per JESD51
Power Dissipation	MSOP8 0.15" SOIC8 0.3" SOIC16 PDIP8	P_D			500 675 1500 800	mW	

Notes (apply to both 3.3 V and 5 V specifications):

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
4. CM_H and CM_L are the maximum common mode voltage slew rates that can be applied with the outputs remaining stable and within V_{OL} and V_{OH} specifications.
5. Device is considered a two terminal device: pins 1–4 shorted and pins 5–8 shorted.
6. Dynamic power consumption is calculated per channel.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 9.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 9).
10. 64k-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

Typical Performance Graphs

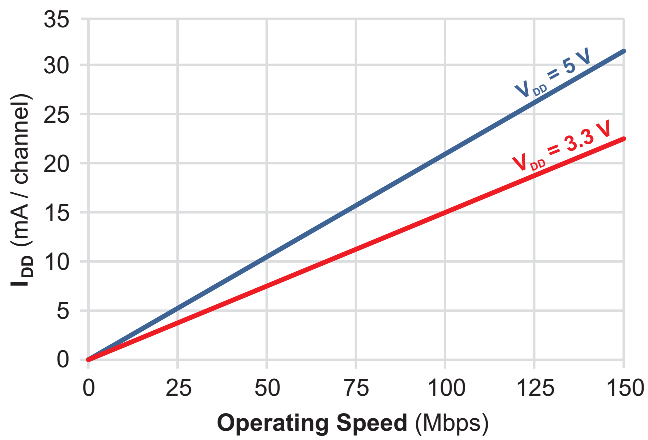


Figure 1. Supply current (per channel) vs. operating speed.

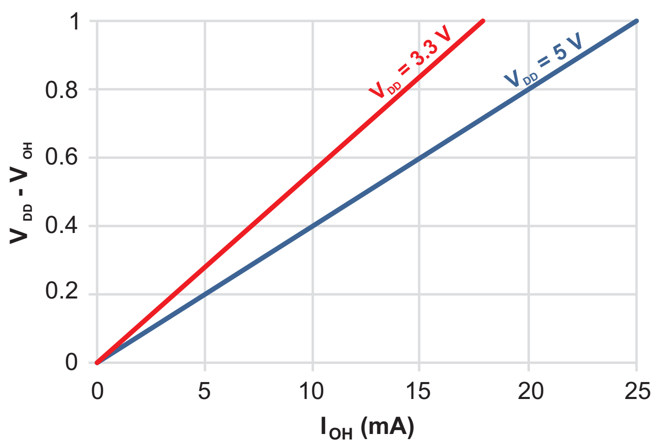


Figure 2. Typical high output voltage vs. load.

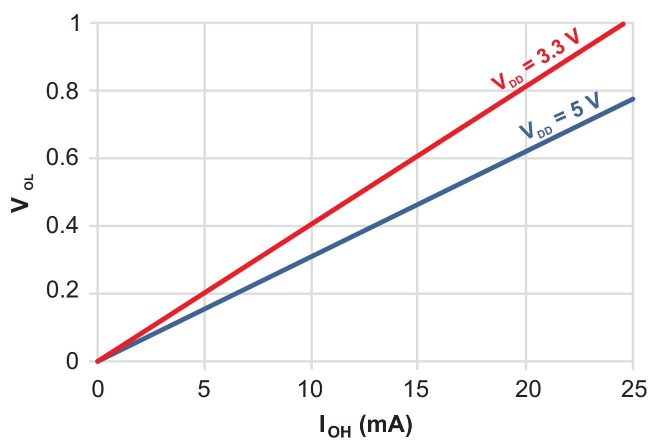


Figure 3. Typical low output voltage vs. load

Application Information

Isolator Operation

An equivalent circuit is shown below:

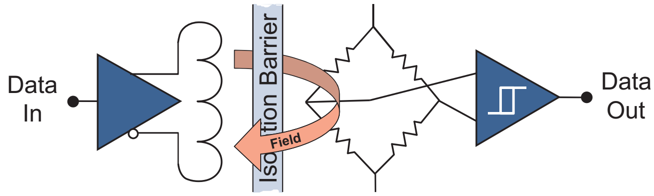


Figure 4. IL711 / IL712 / IL721 equivalent circuit (each channel).

Isolator Signal Path

The GMR isolator signal path starts with a buffered input signal that is driven through an ultraminiature coil. This generates a small magnetic field that changes the electron spin polarization of GMR resistors, which are configured as a Wheatstone bridge. The change in spin polarization of the resistors creates a bridge voltage which drives an output comparator to construct an isolated version of the input signal.

Small Size, High Speed, and Low EMI

The coil, GMR, and circuitry are integrated to allow small packages. GMR is inherently high speed and low distortion, and unlike transformers, does not rely on energy transfer, so power is low and EMI emissions are minimal.

High Magnetic Immunity

GMR provides large signals which improve magnetic immunity, and the Wheatstone bridge configuration cancels ambient common-mode magnetic fields, further enhancing immunity to external magnetic fields.

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Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

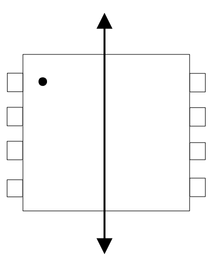
Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:

Cross-axis Field Direction



Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

Power Supply Decoupling

Both power supplies should be decoupled with 0.1 µF typical (0.047 µF minimum) capacitors as close as possible to the V_{DD} pins. Ground planes for both GND_1 and GND_2 are highly recommended for data rates above 10 Mbps.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Unless the circuit connected to the isolator performs its own power- on reset (POR), a start-up initialization circuit should be considered. Initialization consists of toggling the input either high then low, or low then high.

In CAN applications, the IL712 or IL721 should be used with CAN transceivers with Dominant Timeout functions for seamless POR. Most CAN transceivers have Dominant Timeout options. Examples include NXP's TJA 1050 and TJA 1040 transceivers.

Data Transmission Rates

The reliability of a transmission system is directly related to the accuracy and quality of the transmitted digital information. For a digital system, those parameters which determine the limits of the data transmission are pulse width distortion and propagation delay skew.

Propagation delay is the time taken for the signal to travel through the device. This is usually different when sending a low-to-high than when sending a high-to-low signal. This difference, or error, is called pulse width distortion (PWD) and is usually in nanoseconds. It may also be expressed as a percentage:

$$\text{PWD\%} = \frac{\text{Maximum Pulse Width Distortion (ns)}}{\text{Signal Pulse Width (ns)}} \times 100\%$$

For example, with data rates of 12.5 Mbps:

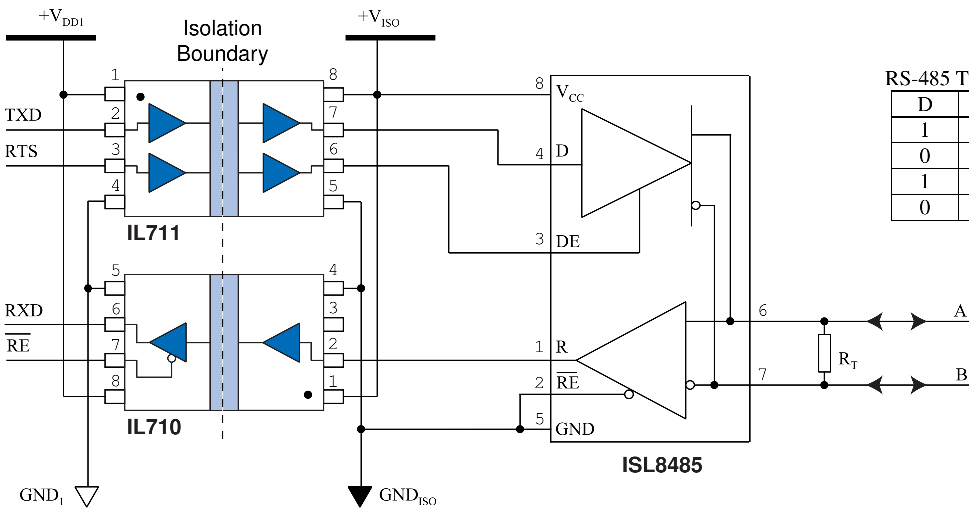
$$\text{PWD\%} = \frac{3\text{ ns}}{80\text{ ns}} \times 100\% = 3.75\%$$

This figure is almost **three times** better than any available optocoupler with the same temperature range, and **two times** better than any optocoupler regardless of published temperature range. IsoLoop isolators exceed the 10% maximum PWD recommended by PROFIBUS, and will run to nearly 35 Mb within the 10% limit.

Propagation delay skew is the signal propagation difference between two or more channels. This becomes significant in clocked systems because it is undesirable for the clock pulse to arrive before the data has settled. Propagation delay skew is especially critical in high data rate parallel systems for establishing and maintaining accuracy and repeatability. Worst-case channel-to-channel skew in an IL700 Isolator is just 3 ns—**ten times** better than any optocoupler. IL700 Isolators have a maximum propagation delay skew of 6 ns—**five times** better than any optocoupler.

Illustrative Applications

NVE offers a unique line of single-chip isolated RS-485, PROFIBUS, and CAN transceivers, but as illustrated in the circuits below, IL700-Series Isolators can also be used as part of multi-chip designs with non-isolated transceivers:



RS-485 Truth Table

D	DE	A	B	R
1	0	Z	Z	X
0	0	Z	Z	X
1	1	1	0	1
0	1	0	1	0

Figure 1. Isolated PROFIBUS / RS-485 circuit.

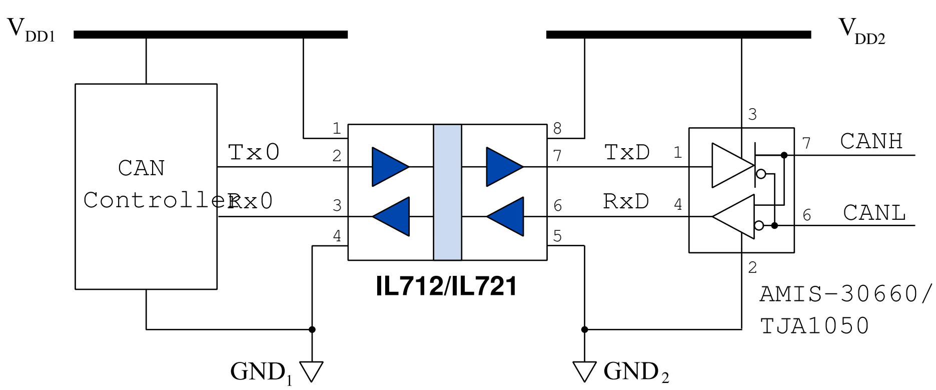


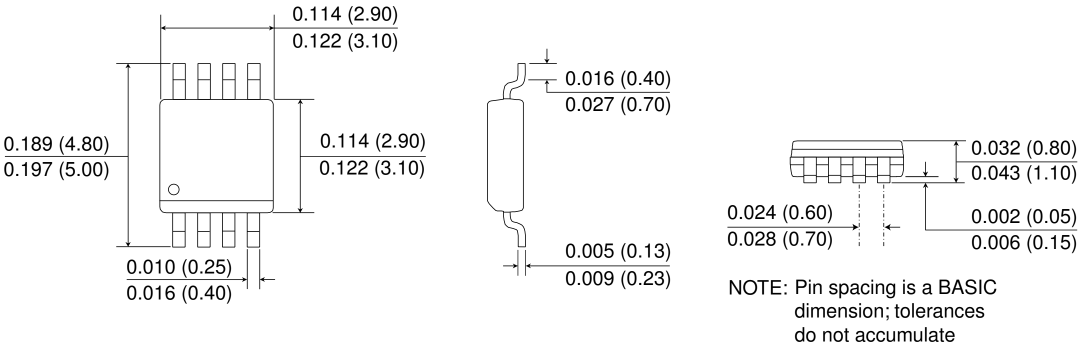
Figure 2. Isolated CAN circuit.

CAN isolation is increasingly necessary to reduce EMI susceptibility, especially in high- speed applications and in hybrid and electrical vehicle networks, where the 12 V battery has been replaced with one of several hundred volts. Operator and equipment safety becomes critical when a high voltage source, such as the battery, needs to be connected to diagnosis systems during routine maintenance procedures. In the application shown above, the microcontroller is isolated from the CAN transceiver by an IL712 or IL721, allowing higher speed and more reliable bus operation by eliminating ground loops and reducing susceptibility to noise and EMI events. The best-in-class 10 ns typical IL712/IL721 propagation delay minimizes CAN loop delay and maximizes data rate over any given bus length. This simple circuit works with any CAN transceiver with a TxD dominant timeout, which includes all of the current-generation transceivers.

Package Drawings

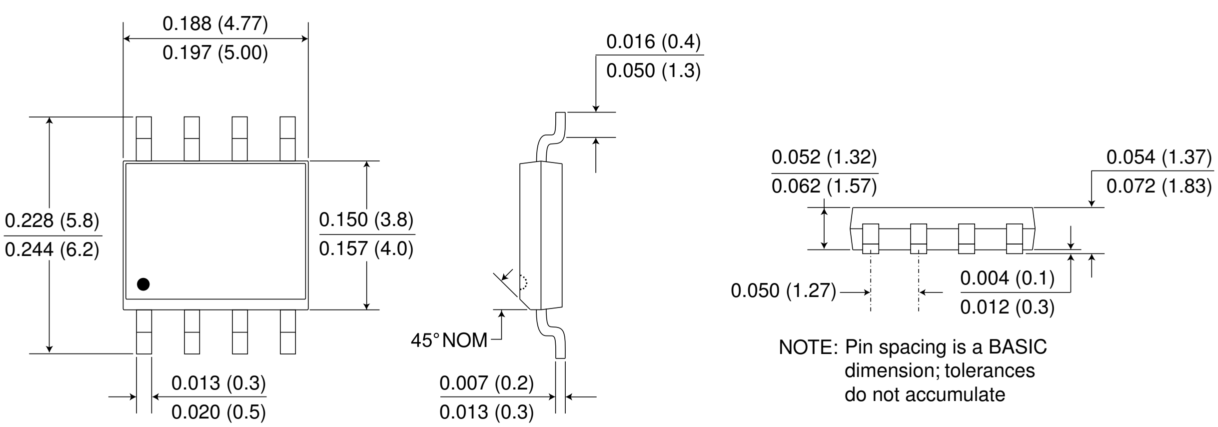
8-pin MSOP (-1 suffix)

Dimensions in inches (mm); scale = approx. 5X



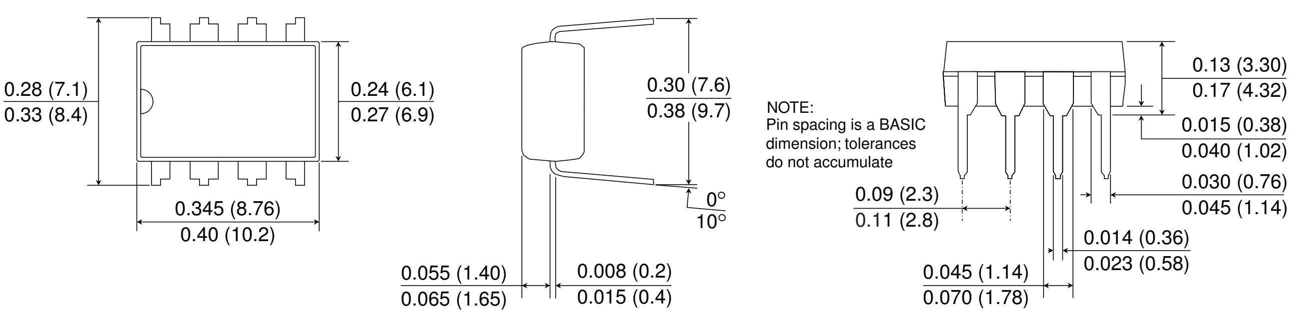
8-pin SOIC Package (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X



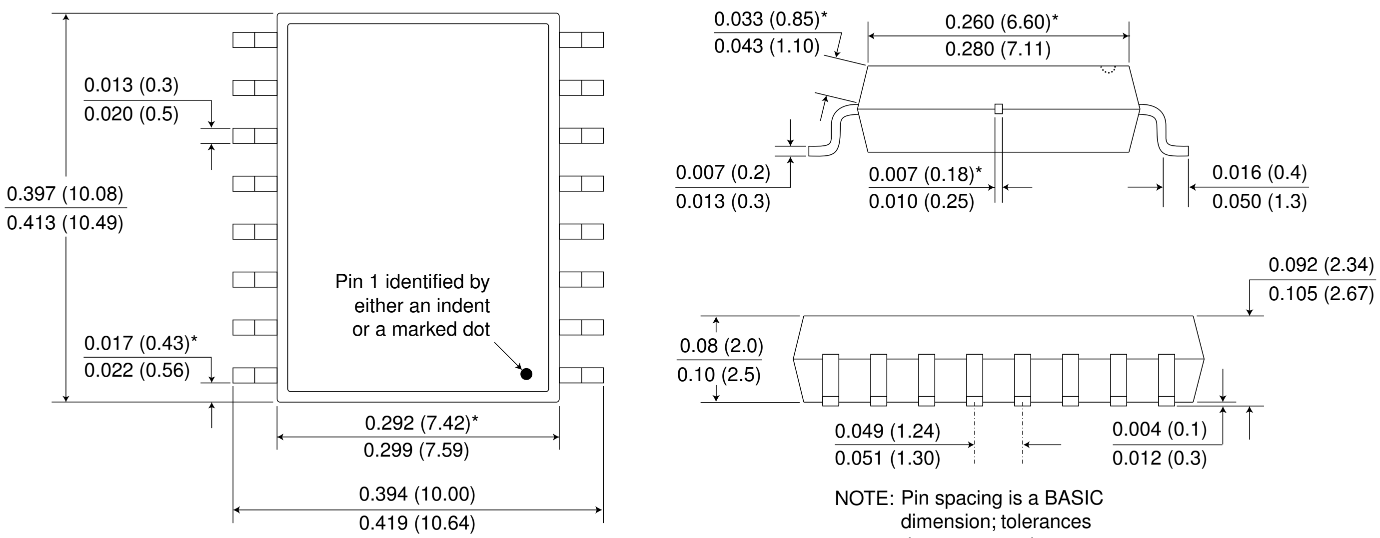
8-pin PDIP (-2 suffix)

Dimensions in inches (mm); scale = approx. 2.5X



True 8™ (8 mm creepage) 16-pin SOIC Package (no suffix)

Dimensions in inches (mm); scale = approx. 5X



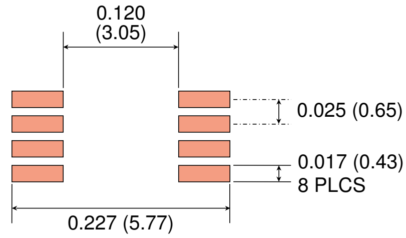
NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layouts

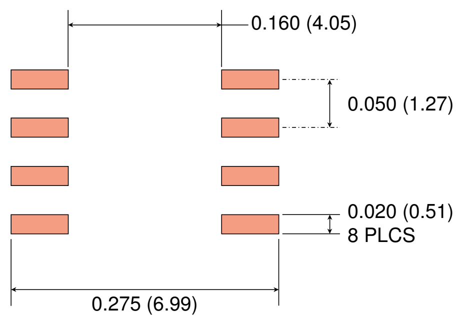
8-pin MSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X



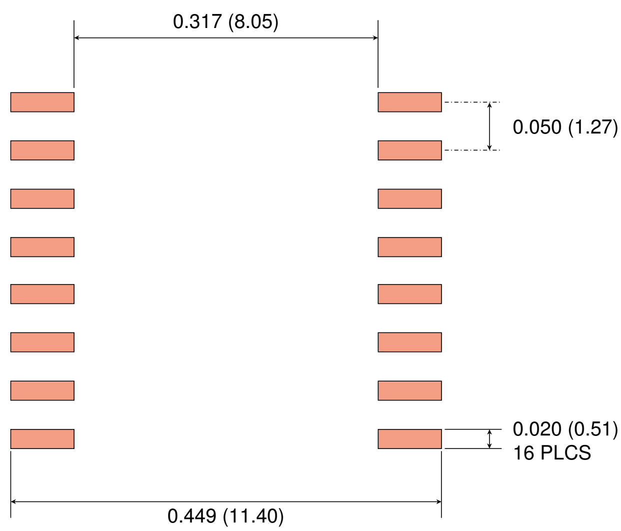
8-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



True 8™ 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



Ordering Information

IL 711 T - 3 E TR13

Bulk Packaging (TR13)
- Blank = Tube
- TR7 = 7" Tape and Reel
- TR13 = 13" Tape and Reel

Package (E)
- Blank = 80/20 Tin/Lead Plating
- E = RoHS Compliant

Package Type (3)
- -1 = MSOP
- -2 = PDIP
- -3 = 0.15" 8-pin SOIC
- Blank = True 8 (8mm creepage)

Grade (T)
- Blank = Standard
- S = High Speed (150 Mbps)
- T = High Temperature (125˚C)
- V = High Isolation Voltage (6 kV True 8; 2.5 kV MSOP)

Base Part Number (711)
- 711 = 2 Transmit Channels
- 712 = 1 Transmit Channel, 1 Receive Channel
- 721 = 1 Transmit Channel, 1 Receive Channel (reverse pinout)

Product Family (IL)
- IL = Isolators

Valid Part Numbers

IL711E	IL712-1E	IL721E
IL711TE	IL712S-1E	IL721TE
IL711VE	IL712T-1E	IL721VE
	IL712TV-1E	
IL711-1E	IL712V-1E	IL721-3
IL711S-1E		IL721-3E
IL711T-1E	IL712-2	IL721T-3
IL711TV-1E	IL712-2E	IL721T-3E
IL711V-1E	IL712T-2	
	IL712T-2E	
IL711-2		
IL711-2E	IL712-3	
IL711T-2	IL712S-3	
IL711T-2E	IL712T-3	
	IL712-3E	
IL711-3	IL712S-3E	
IL711S-3	IL712T-3E	
IL711T-3		
IL711-3E		
IL711S-3E		
IL711T-3E		

All MSOP and SOIC parts are available on tape and reel.

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Available Parts

Available Parts	Transmit Channels	Receive Channels	Mbps	Maximum Temperature	Isolation Voltage (RMS)	Package	RoHS
IL711-1E	2	0	110	100°C	1 kV	MSOP-8	Y
IL711-2	2	0	110	100°C	2.5 kV	PDIP-8	N
IL711-2E	2	0	110	100°C	2.5 kV	PDIP-8	Y
IL711-3	2	0	110	100°C	2.5 kV	SOIC-8	N
IL711-3E	2	0	110	100°C	2.5 kV	SOIC-8	Y
IL711S-1E	2	0	150	100°C	1 kV	MSOP-8	Y
IL711S-3E	2	0	150	100°C	2.5 kV	SOIC-8	Y
IL711T-1E	2	0	110	125°C	1 kV	MSOP-8	Y
IL711TV-1E	2	0	110	125°C	2.5 kV	MSOP-8	Y
IL711T-2	2	0	110	125°C	2.5 kV	PDIP-8	N
IL711T-2E	2	0	110	125°C	2.5 kV	PDIP-8	Y
IL711T-3	2	0	110	125°C	2.5 kV	SOIC-8	N
IL711T-3E	2	0	110	125°C	2.5 kV	SOIC-8	Y
IL711V-1E	2	0	110	100°C	2.5 kV	MSOP-8	Y
IL711VE	2	0	110	125°C	6 kV	True8	Y
IL712-1E	1	1	110	100°C	1 kV	MSOP-8	Y
IL712-2	1	1	110	100°C	2.5 kV	PDIP-8	N
IL712-2E	1	1	110	100°C	2.5 kV	PDIP-8	Y
IL712-3	1	1	110	100°C	2.5 kV	SOIC-8	N
IL712-3E	1	1	110	100°C	2.5 kV	SOIC-8	Y
IL712S-1E	1	1	150	100°C	1 kV	MSOP-8	Y
IL712S-3E	1	1	150	100°C	2.5 kV	SOIC-8	Y
IL712T-1E	1	1	110	125°C	1 kV	MSOP-8	Y
IL712TV-1E	1	1	110	125°C	2.5 kV	MSOP-8	Y
IL712T-2	1	1	110	125°C	2.5 kV	PDIP	N
IL712T-2E	1	1	110	125°C	2.5 kV	PDIP	Y
IL712T-3	1	1	110	125°C	2.5 kV	SOIC-8	N
IL712T-3E	1	1	110	125°C	2.5 kV	SOIC-8	Y
IL712V-1E	1	1	110	100°C	2.5 kV	MSOP	Y
IL721-3E	1	1	110	105°C	2.5 kV	SOIC-8	Y
IL721E	1	1	110	100°C	2.5 kV	True8	Y
IL721T-3E	1	1	110	125°C	2.5 kV	SOIC-8	Y
IL721VE	1	1	110	125°C	6 kV	True8	Y

All MSOP and SOIC part types are available on tape and reel.

ISB-DS-001-IL711/12-AO
November 2020

Change

- Changed “Propagation Delay Skew” to “Propagation Delay difference between any two parts” for clarity (pp. 6 and 7).
- Added output-side dynamic current specifications (pp. 6 and 7).

ISB-DS-001-IL711/12-AN

Changes

- Upgraded CMTI specifications.
- Added ATEC / IEC 60079 Intrinsic Safety pending (p. 3).

ISB-DS-001-IL711/12-AM

Changes

- Extended minimum operating power supplies to 2.7 volts.
- Explicitly listed part types for max. operating temperatures.
- Changed PDIP8 creepage specifications from 7.04 mm to 6.8 mm.
- Updated EMC standards.
- Deleted minimum magnetic field immunity specifications (not 100% tested).
- Revised thermal resistance specifications.
- Added Typical Performance Graphs.
- More detailed description of operation.

ISB-DS-001-IL711/12-AL

Changes

- Added IL711TV-1E and IL712TV-1E
  125°C, 2.5 kV isolation MSOP configurations.
- Eliminated non-RoHS MSOPs.

ISB-DS-001-IL711/12-AK

Change

- Updated SOIC8 package outline drawing.

ISB-DS-001-IL711/12-AJ

Change

- Updated VDE Reinforced Isolation file number and description.

ISB-DS-001-IL711/12-AI

Changes

- Updated VDE certification standard to VDE V 0884-10.
- Upgraded “VE” Version Surge Immunity specification to 12.8 kV.
- Upgraded “VE” Version VDE 0884-10 rating to reinforced insulation.

ISB-DS-001-IL711/12-AH

Changes

- Increased V-Series isolation voltage to 6 kVrms.
- Increased typ. Total Barrier Thickness specification to 0.016 mm.
- Increased CTI min. specification to ≥600 V_{RMS}.

ISB-DS-001-IL711/12-AG

Changes

- Added V-Series high isolation voltage versions (5 kV True 8 and 2.5 kV MSOP).
- More detailed “Available Parts” table.

ISB-DS-001-IL711/12-AF

Changes

- Added product illustrations to first page.
- Revised and added details to thermal characteristic specifications (p. 2).
- Added VDE 0884 Safety-Limiting Values (p. 3).

ISB-DS-001-IL711/12-AE

Changes

- IEC 60747-5-5 (VDE 0884) certification.

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Limiting Values
Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the recommended operating conditions of the datasheet is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

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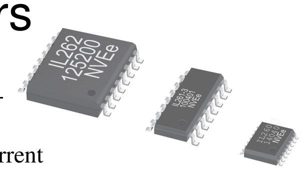
ISB-DS-001-IL711/12-AO

November 2020

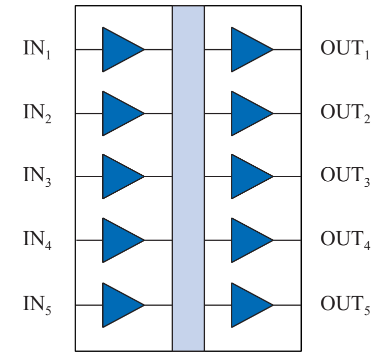
NVE CORPORATION

IL260/IL261/IL262

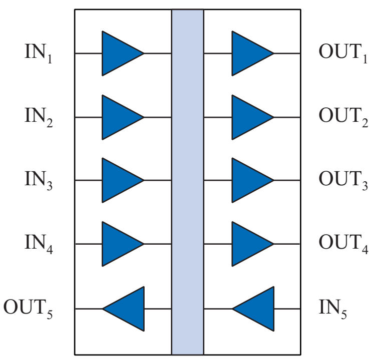
High Speed Five-Channel Digital Isolators



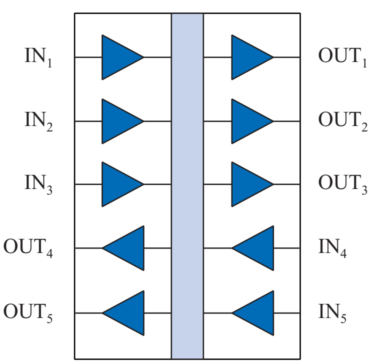
Functional Diagrams



IL260



IL261



IL262

Features

- High Speed: 110 Mbps
- 1.2 mA/channel typical quiescent current
- Very high isolation: 6 kV_{RMS} Reinforced Isolation (V-Series)
- 50 kV/µs typ.; 30 kV/µs min. common mode transient immunity
- No carrier or clock for low EMI emissions and susceptibility
- −40 °C to 85 °C operating temperature
- 44000 year barrier life
- Excellent magnetic immunity
- 2 ns typical pulse width distortion
- 100 ps pulse jitter
- 4 ns typical propagation delay skew
- 10 ns typical propagation delay
- 2 ns channel-to-channel skew
- VDE certified; UL 1577 recognized
- 0.15" and True 8™ mm 16-pin SOIC; 16-pin QSOP packages

Applications

- ADCs and DACs
- Multiplexed data transmission
- Board-to-board communication
- Peripheral interfaces
- Equipment covered under IEC 61010-1 Edition 3
- 5 kV_{RMS} rated IEC 60601-1 medical applications

Description

NVE's IL260-Series five-channel high-speed digital isolators are CMOS devices manufactured with NVE's patented* IsoLoop® spintronic Giant Magnetoresistive (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

All transmit and receive channels operate at 110 Mbps over the full temperature and supply voltage range. The symmetric magnetic coupling barrier provides a typical propagation delay of only 10 ns and a pulse width distortion of 2 ns, achieving the best specifications of any isolator. The unique fifth channel can be is used to distribute isolated clocks or handshake signals to multiple delta-sigma A/D converters. High channel density makes these devices ideal for isolating ADCs and DACs, parallel buses and peripheral interfaces.

Typical transient immunity of 50 kV/µs is unsurpassed. Performance is specified over the temperature range of −40 °C to +85 °C without derating.

The five-channel devices provide the highest channel density available. Parts are available in ultraminiature 16-pin QSOPs, as well as 0.15"and 0.3"-wide SOIC packages.

V-Series versions offer extremely high isolation voltage of 6 kV_{RMS}, and true 8 mm creepage.

*U.S. Patent number 5,831,426; 6,300,617 and others.

REV. W

Absolute Maximum Ratings[1]

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage Temperature	T_S	–55		150	°C	
Junction Temperature	T_J	–55		150	°C	
Ambient Operating Temperature	T_A	–40		85	°C	
Supply Voltage	V_{DD1},V_{DD2}	–0.5		7	V	
Input Voltage	V_I	–0.5		V_{DD} + 0.5	V	
Output Voltage	V_O	–0.5		V_{DD} + 0.5	V	
Output Current Drive	I_O	–10		10	mA	
Lead Solder Temperature				260	°C	10 sec.
ESD			2		kV	HBM

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Ambient Operating Temperature	T_A	–40		85	°C	
Junction Temperature	T_J	–40		110	°C	
Supply Voltage	V_{DD1},V_{DD2}	2.5		5.5	V	
Logic High Input Voltage	V_{IH}	2.4		V_{DD}	V	
Logic Low Input Voltage	V_{IL}	0		0.8	V	
Input Signal Rise and Fall Times	t_{IR}, t_{IF}			1	μs	

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Safety and Approvals

VDE V 0884-10 (VDE V 0884-11 pending)

V-Series (Reinforced Isolation; VDE File Number 5016933-4880-0002)

- Working Voltage (V_{IORM}) 1000 V_{RMS} (1415 V_{PK}); reinforced insulation; pollution degree 2
- Isolation voltage (V_{ISO}) 6000 V_{RMS}
- Surge immunity (V_{IOSM}) 12.8 kV_{PK}
- Surge rating 8 kV
- Transient overvoltage (V_{IOTM}) 6000 V_{PK}
- Each part tested at 2387 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 6000 V_{PK} for 60 sec.; then 2122 V_{PK} for 10 sec. with 5 pC partial discharge limit

Standard versions (Basic Isolation; VDE File Number 5016933-4880-0001)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Isolation voltage (V_{ISO}) 2500 V_{RMS}
- Transient overvoltage (V_{IOTM}) 4000 V_{PK}
- Surge rating 4000 V
- Each part tested at 1590 V_{PK} for 1 second, 5 pC partial discharge limit
- Samples tested at 4000 V_{PK} for 60 sec.; then 1358 V_{PK} for 10 sec. with 5 pC partial discharge limit

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180°C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)

Reinforced Insulation; Pollution Degree II; Material Group III

Part No. Suffix	Package	Working Voltage
-1	QSOP	300 V_{RMS}
-3	0.15" SOIC	300 V_{RMS}
None	0.3" SOIC (standard)	300 V_{RMS}
V	0.3" SOIC (high isolation voltage)	1000 V_{RMS}

UL 1577 (Component Recognition Program File Number E207481)

V-Series isolation grade

6 kV rating; tested at 7.2 kV_{RMS} (10.2 kV_{PK}) for 1 second; each lot sample tested at 6 kV_{RMS} (8485 V_{PK}) for 1 minute

Standard isolation grade

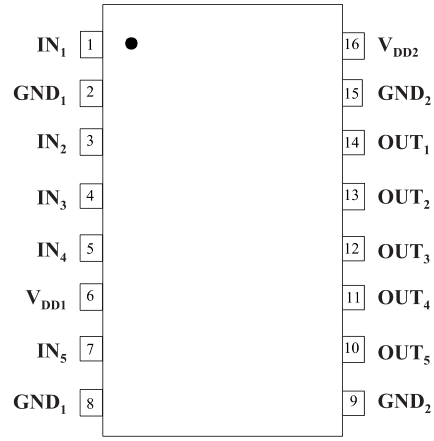
Each part tested at 3000 V_{RMS} (4243 V_{PK}) for 1 second; each lot sample tested at 2500 V_{RMS} (3536 V_{PK}) for 1 minute

Soldering Profile

Per JEDEC J-STD-020C, MSL 1

IL260 Pin Connections

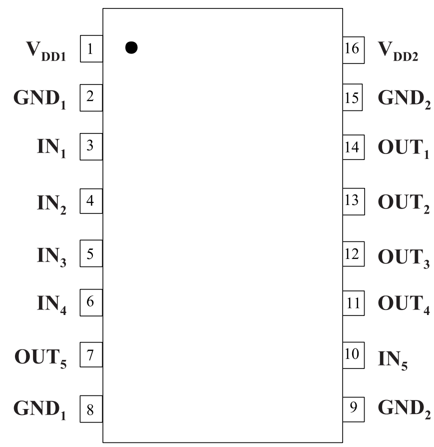
1	IN_1	Input 1
2	GND_1	Ground*
3	IN_2	Input 2
4	IN_3	Input 3
5	IN_4	Input 4
6	V_{DD1}	Supply Voltage 1
7	IN_5	Input 5
8	GND_1	Ground*
9	GND_2	Ground*
10	OUT_5	Output 5
11	OUT_4	Output 4
12	OUT_3	Output 3
13	OUT_2	Output 2
14	OUT_1	Output 1
15	GND_2	Ground*
16	V_{DD2}	Supply Voltage 2



IL260

IL261 Pin Connections

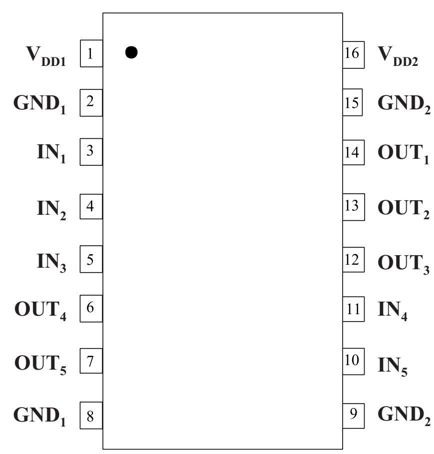
1	V_{DD1}	Supply Voltage 1
2	GND_1	Ground*
3	IN_1	Input 1
4	IN_2	Input 2
5	IN_3	Input 3
6	IN_4	Input 4
7	OUT_5	Output 5
8	GND_1	Ground*
9	GND_2	Ground*
10	IN_5	Input 5
11	OUT_4	Output 4
12	OUT_3	Output 3
13	OUT_2	Output 2
14	OUT_1	Output 1
15	GND_2	Ground*
16	V_{DD2}	Supply Voltage 2



IL261

IL262 Pin Connections

1	V_{DD1}	Supply Voltage 1
2	GND_1	Ground*
3	IN_1	Input 1
4	IN_2	Input 2
5	IN_3	Input 3
6	OUT_4	Output 4
7	OUT_5	Output 5
8	GND_1	Ground*
9	GND_2	Ground*
10	IN_5	Input 5
11	IN_4	Input 4
12	OUT_3	Output 3
13	OUT_2	Output 2
14	OUT_1	Output 1
15	GND_2	Ground*
16	V_{DD2}	Supply Voltage 2



IL262

***NOTE:** Pins 2 and 8 are internally connected, as are pins 9 and 15.

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3.3 Volt Electrical Specifications (T_{min} to T_{max})						
Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Current IL260	I_{DD1}		300	400	µA	
Input Quiescent Current IL261	I_{DD1}		1.2	1.75	mA	
Input Quiescent Current IL262	I_{DD1}		2.4	3.5	mA	
Output Quiescent Current IL260	I_{DD2}		6	8.75	mA	
Output Quiescent Current IL261	I_{DD2}		4.8	7	mA	
Output Quiescent Current IL262	I_{DD2}		3.6	5.25	mA	
Logic Input Current	I_i	−10		10	µA	
Logic High Output Voltage	V_{OH}	V_{DD}−0.1	V_{DD}		V	$I_O = -20$ µA, $V_I=V_{IH}$
		0.8 x V_{DD}	0.9 x V_{DD}		V	$I_O = -4$ mA, $V_I=V_{IH}$
Logic Low Output Voltage	V_{OL}		0	0.1	V	$I_O = 20$ µA, $V_I=V_{IL}$
			0.5	0.8	V	$I_O = 4$ mA, $V_I=V_{IL}$

Switching Specifications (2.5 V < V_{DD} < 3.6 V)						
Maximum Data Rate		100	110		Mbps	$C_L = 15$ pF
Minimum Pulse Width[7]	PW	10			ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		12	18	ns	$C_L = 15$ pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		12	18	ns	$C_L = 15$ pF
Pulse Width Distortion $\lvert t_{PHL}-t_{PLH}\rvert$[2]	PWD		2	3	ns	$C_L = 15$ pF
Propagation Delay Skew[3]	t_{PSK}		4	6	ns	$C_L = 15$ pF
Output Rise Time (10%–90%)	t_R		2	4	ns	$C_L = 15$ pF
Output Fall Time (10%–90%)	t_F		2	4	ns	$C_L = 15$ pF
Common Mode Transient Immunity (Output Logic High to Logic Low)[4]	$\lvert CM_H\rvert$,$\lvert CM_L\rvert$	30	50		kV/µs	$V_{CM} = 1500$ V_{DC} $t_{TRANSIENT} = 25$ ns
Channel-to-Channel Skew			2	3	ns	$C_L = 15$ pF
Dynamic Power Consumption[6]			140	240	µA/Mbps	per channel

Magnetic Field Immunity[8] ($V_{DD2} = 3$ V, 3 V < V_{DD1} < 5.5 V)						
Power Frequency Magnetic Immunity	H_{PF}		1500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		2000		A/m	$t_p = 8$µs
Damped Oscillatory Magnetic Field	H_{OSC}		2000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

5 Volt Electrical Specifications (T_{min} to T_{max})							
Parameters		**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Quiescent Current	IL260	I_{DD1}		350	500	µA	
	IL261			1.8	2.5	mA	
	IL262			3.6	5	mA	
Output Quiescent Current	IL260	I_{DD2}		9	12.5	mA	
	IL261			7.2	10	mA	
	IL262			5.4	7.5	mA	
Logic Input Current		I_i	−10		10	µA	
Logic High Output Voltage		V_{OH}	V_{DD}−0.1	V_{DD}		V	$I_O = -20$ µA, $V_I = V_{IH}$
			0.8 x V_{DD}	0.9 x V_{DD}			$I_O = -4$ mA, $V_I = V_{IH}$
Logic Low Output Voltage		V_{OL}		0	0.1	V	$I_O = 20$ µA, $V_I = V_{IL}$
				0.5	0.8		$I_O = 4$ mA, $V_I = V_{IL}$

Switching Specifications (V_{DD} = 5 V)						
Maximum Data Rate		100	110		Mbps	C_L = 15 pF
Minimum Pulse Width[7]	PW	10			ns	50% Points, V_O
Propagation Delay Input to Output (High to Low)	t_{PHL}		10	15	ns	C_L = 15 pF
Propagation Delay Input to Output (Low to High)	t_{PLH}		10	15	ns	C_L = 15 pF
Pulse Width Distortion $\lvert t_{PHL}-t_{PLH}\rvert$[2]	PWD		2	3	ns	C_L = 15 pF
Pulse Jitter[10]	t_J		100		ps	C_L = 15 pF
Propagation Delay Skew[3]	t_{PSK}		4	6	ns	C_L = 15 pF
Output Rise Time (10%–90%)	t_R		1	3	ns	C_L = 15 pF
Output Fall Time (10%–90%)	t_F		1	3	ns	C_L = 15 pF
Common Mode Transient Immunity (Output Logic High to Logic Low)[4]	$\lvert CM_H\rvert,\lvert CM_L\rvert$	30	50		kV/µs	V_{CM} = 1500 V_{DC} $t_{TRANSIENT}$ = 25 ns
Channel-to-Channel Skew			2	3	ns	C_L = 15 pF
Dynamic Power Consumption[6]			200	340	µA/Mbps	per channel

Magnetic Field Immunity[8] (V_{DD2} = 5 V, 3 V < V_{DD1} < 5.5V)						
Power Frequency Magnetic Immunity	H_{PF}		3500		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}		4500		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}		4500		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier[9]	K_X		2.5			

Insulation Specifications

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage Distance (external)	QSOP		4.03			mm	Per IEC 60601
	0.15" SOIC		4.03			mm	
	0.3" SOIC		8.03	8.3		mm	
Total Barrier Thickness (internal)			0.012	0.016		mm	
Leakage Current(5)				0.2		μA_{RMS}	240 V_{RMS}
Barrier Resistance(5)		R_{IO}		$>10^{14}$		Ω	500 V
Barrier Capacitance(5)		C_{IO}		5		pF	f = 1 MHz
Comparative Tracking Index		CTI	≥600			V_{RMS}	Per IEC 60112
High Voltage Endurance (Maximum Barrier Voltage for Indefinite Life)	AC	V_{IO}	1000			V_{RMS}	At maximum operating temperature
	DC	V_{IO}	1500			V_{DC}	
Surge Immunity ("V" Versions)		V_{IOSM}	12.8			kV_{PK}	Per IEC 61000-4-5
Barrier Life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	QSOP	θ_{JA}		100		°C/W	Double-sided PCB in free air
	0.15" SOIC16			82			
	0.3" SOIC16			67			
Junction–Case (Top) Thermal Resistance	QSOP	θ_{JC}		9		°C/W	Double-sided PCB in free air
	0.15" SOIC16			8			
	0.3" SOIC16			12			
Junction–Ambient Thermal Resistance	0.3" SOIC	θ_{JA}		46		°C/W	2s2p PCB in free air per JESD51
Junction–Case (Top) Thermal Resistance	0.3" SOIC	θ_{JC}		9		°C/W	2s2p PCB in free air per JESD51
Power Dissipation	QSOP	P_D			675	mW	
	0.15" SOIC16				675		
	0.3" SOIC16				1500		

Notes:

1. Absolute maximum means the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD is equal to PWD divided by pulse width.
3. t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between devices at 25°C.
4. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common mode input voltage that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
5. Device is considered a two terminal device: pins 1–8 shorted and pins 9–16 shorted.
6. Dynamic power consumption numbers are calculated per channel and are supplied by the channel's input side power supply.
7. Minimum pulse width is the minimum value at which specified PWD is guaranteed.
8. The relevant test and measurement methods are given in the Electromagnetic Compatibility section on p. 8.
9. External magnetic field immunity is improved by this factor if the field direction is "end-to-end" rather than to "pin-to-pin" (see diagram on p. 8).
10. 66,535-bit pseudo-random binary signal (PRBS) NRZ bit pattern with no more than five consecutive 1s or 0s; 800 ps transition time.

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Application Information

Electrostatic Discharge Sensitivity

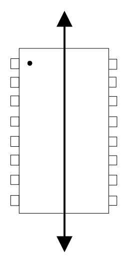
This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

IsoLoop Isolators have the lowest EMC footprint of any isolation technology. There are no internal clocks or carriers. IsoLoop Isolators' Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards.

These isolators are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 standards for immunity, and IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

Immunity to external magnetic fields is even higher if the field direction is "end-to-end" rather than to "pin-to-pin" as shown in the diagram below:



Cross-axis Field Direction

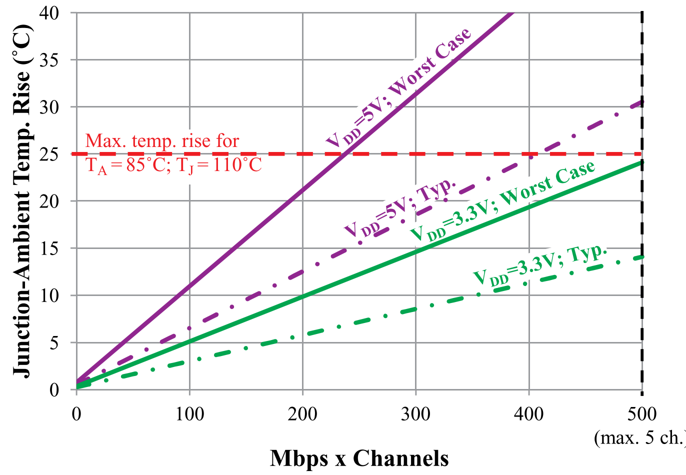
Dynamic Power Consumption

IsoLoop Isolators achieve their low power consumption from the way they transmit data across the isolation barrier. By detecting the edge transitions of the input logic signal and converting these to narrow current pulses, a magnetic field is created around the GMR Wheatstone bridge. Depending on the direction of the magnetic field, the bridge causes the output comparator to switch following the input logic signal. Since the current pulses are narrow, about 2.5 ns, the power consumption is independent of mark-to-space ratio and solely dependent on frequency. This has obvious advantages over optocouplers, which have power consumption heavily dependent on mark-to-space ratio.

Thermal Management

IsoLoop Isolators are designed for low power dissipation and thermal performance, providing unmatched channel density for high-performance isolators. Nevertheless, package temperature rise should be considered when running multiple channels at high speed. Power consumption is higher at 5 volt operation than at 3.3 volts, and dynamic supply current is higher on the input side of the isolators than the output side, so thermal management is more important with five-volt input-side power supplies.

IL260/IL261/IL262 parts have a maximum junction temperature of 110°C. Based on the specifications contained in this datasheet, the derating curve at typical operating conditions is as follows:



Power Supply Decoupling

Both power supplies should be bypassed with 0.1 µF typical (0.047 µF minimum) capacitors as close as possible to the V_{DD} pins. Ground planes for both GND_1 and GND_2 are highly recommended for data rates above 10 Mbps.

Maintaining Creepage

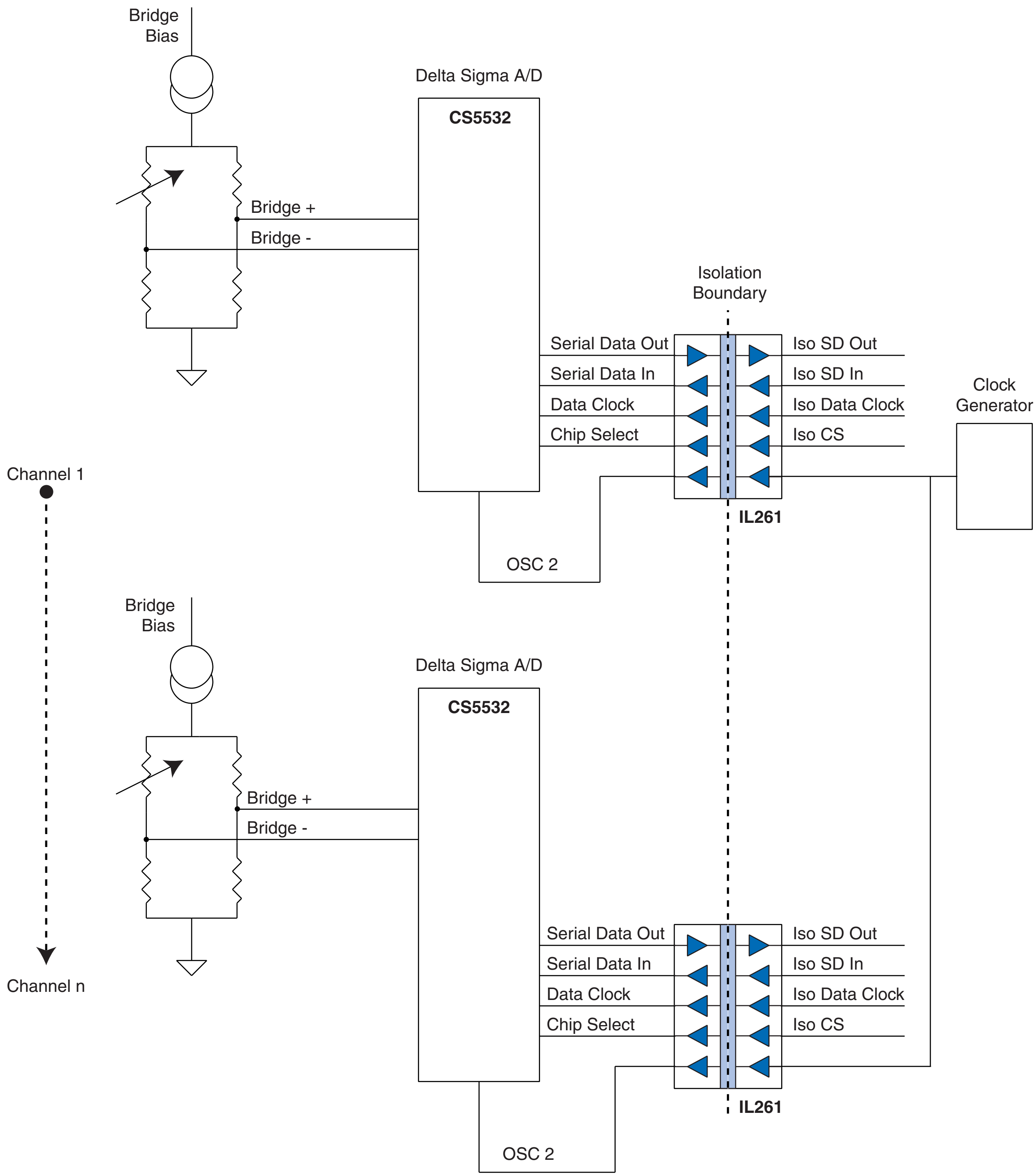
Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Signal Status on Start-up and Shut Down

To minimize power dissipation, input signals are differentiated and then latched on the output side of the isolation barrier to reconstruct the signal. This could result in an ambiguous output state depending on power up, shutdown and power loss sequencing. Therefore, the designer should consider including an initialization signal in the start-up circuit. Initialization consists of toggling the input either high then low, or low then high.

Application Diagram—Multi-Channel Delta-Sigma A/D Converter

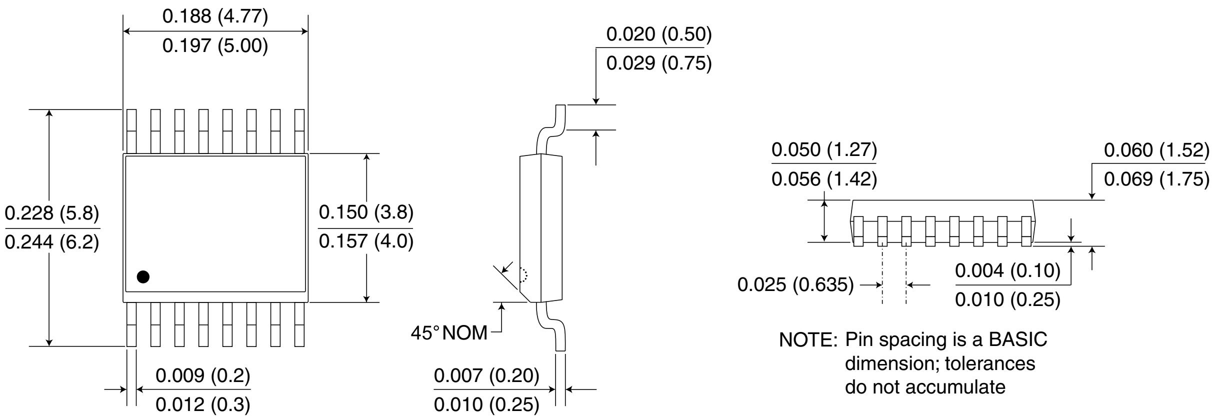
In a typical single-channel delta-sigma ADC, the system clock is located on the isolated side of the system and only four channels of isolation are required. With multiple ADCs configured in a channel-to-channel isolation configuration, however, clock jitter and edge placement accuracy of the system clock must be matched between ADCs. The best solution is to use a single clock on the system side and distribute the clock to each ADC. The five-channel IL261 is ideal, with the fifth channel used to distribute a single, isolated clock to multiple ADCs as shown below:



Package Drawings

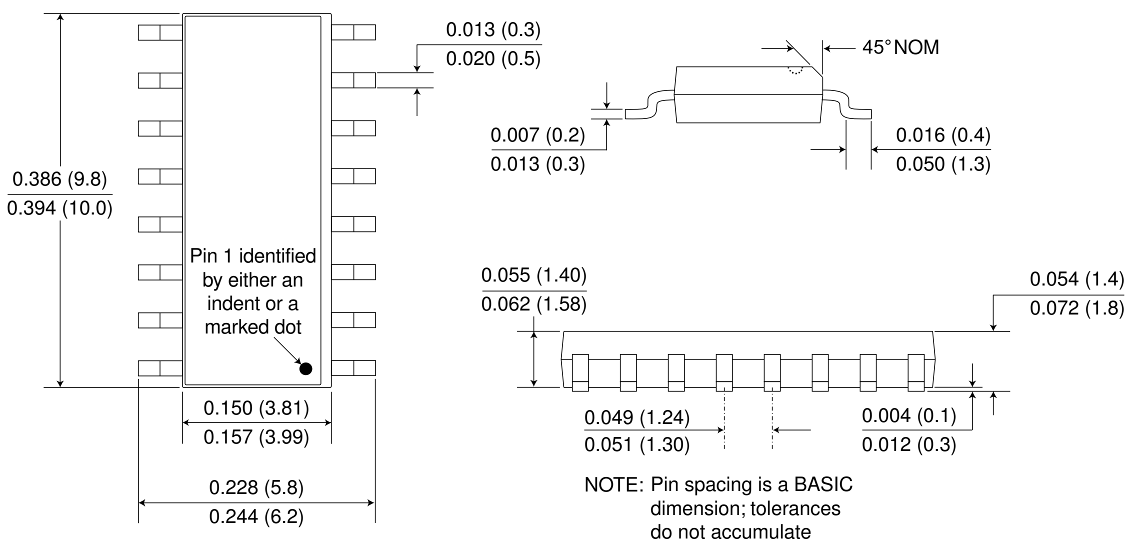
Ultraminiature 16-pin QSOP Package (-1 suffix)

Dimensions in inches (mm); scale = approx. 5X



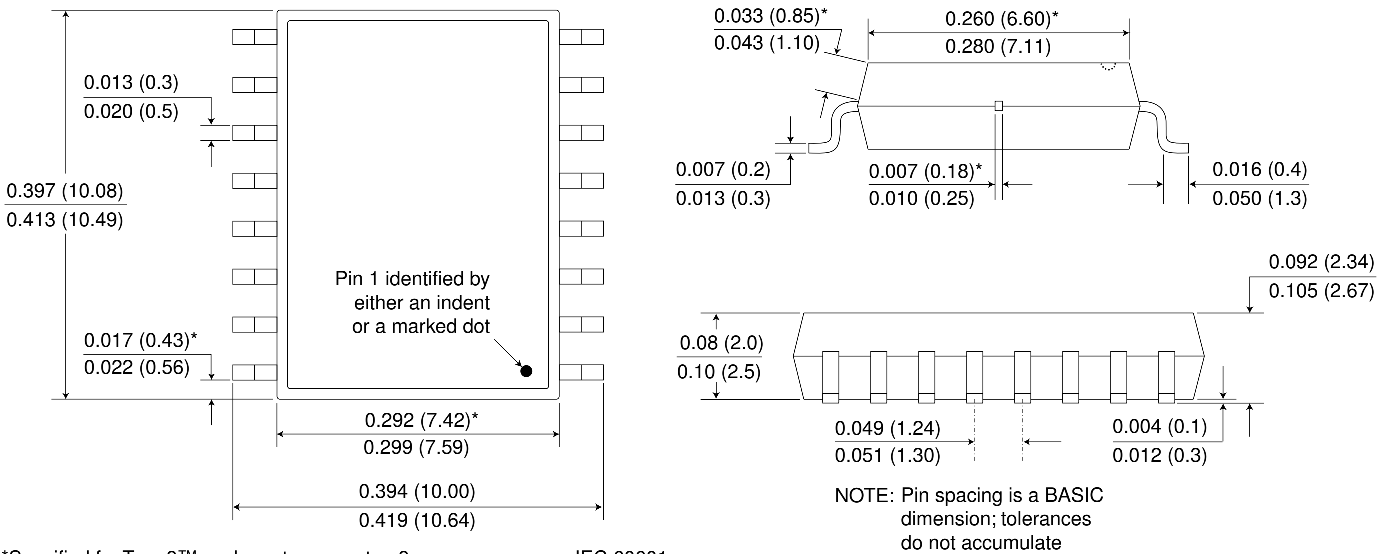
0.15" 16-pin SOIC Package (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X



0.3" 16-pin SOIC Package (no suffix)

Dimensions in inches (mm); scale = approx. 5X

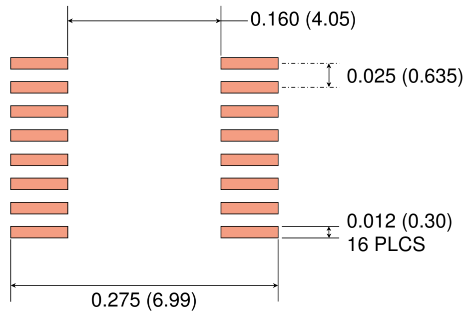


*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layouts

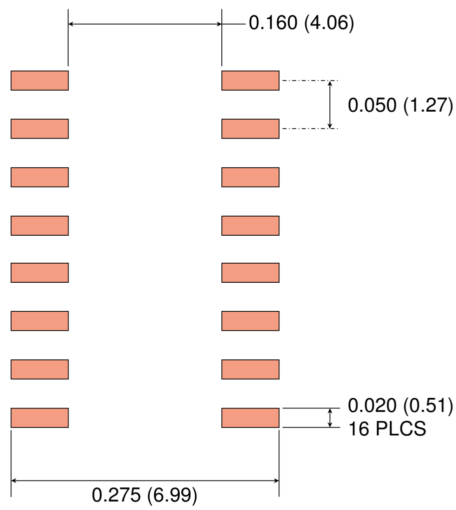
4 mm x 5 mm 16-pin QSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X

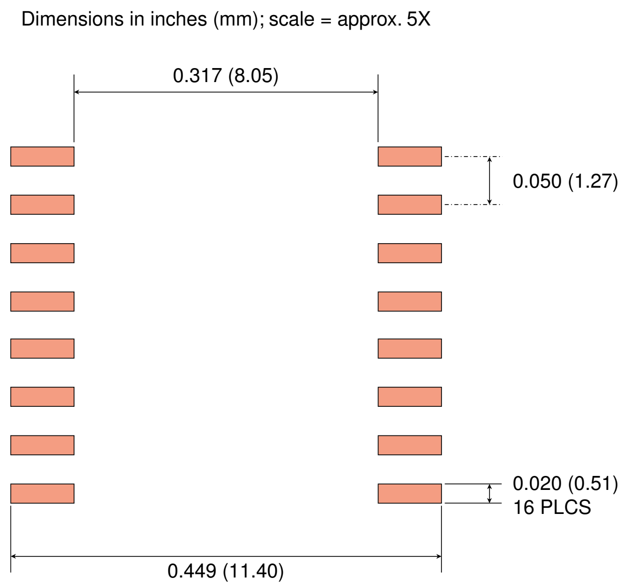


0.15" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X



0.3" 16-pin SOIC Pad Layout



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Available Parts

Available Parts	Transmit Channels	Receive Channels	Isolation Voltage (RMS)	Package
IL260-1E	5	0	2.5 kV	QSOP
IL260-3E	5	0	2.5 kV	Narrow SOIC
IL260E	5	0	2.5 kV	Wide SOIC
IL260VE	5	0	6 kV	Wide SOIC
IL261-1E	4	1	2.5 kV	QSOP
IL261-3E	4	1	2.5 kV	Narrow SOIC
IL261E	4	1	2.5 kV	Wide SOIC
IL261VE	4	1	6 kV	Wide SOIC
IL262-3E	3	2	2.5 kV	Narrow SOIC
IL262E	3	2	2.5 kV	Wide SOIC
IL262VE	3	2	6 kV	Wide SOIC

All part types are available on tape and reel.

Ordering Information

IL 260 V - 3 E TR13

Bulk Package
Blank = Tube
TR7 = 7" Tape and Reel
TR13 = 13" Tape and Reel

Package
Blank = 80/20 Tin/Lead Plating
E = RoHS Compliant

Package Type
Blank = 0.3" 16-pin SOIC
-1 = 0.15" 16-pin QSOP
-3 = 0.15" 16-pin SOIC

Grade
Blank = Standard Isolation Voltage (2.5 kV)
V = High Isolation Voltage (6 kV)

Base Part Number
260 = 5 Transmit Channels
261 = 4 Transmit Channels; 1 Receive Channel
262 = 3 Transmit Channels; 2 Receive Channel

Product Family
IL = Isolators

Valid Part Numbers

IL260
IL260E
IL260VE
IL260-1E
IL260-3
IL260-3E
IL261
IL261E
IL261VE
IL261-1E
IL261-3
IL261-3E
IL262
IL262E
IL262VE
IL262-3
IL262-3E

All IL260-Series part types are available on tape and reel.

RoHS COMPLIANT

NVE Corporation 11409 Valley View Road, Eden Prairie, MN 55344-3617 (952) 829-9217 www.nve.com YouTube.com/NveCorporation iso-apps@nve.com

Revision History

ISB-DS-001-IL260/1/2-W
January 2020

Changes
- Reduced minimum supply voltage to 2.5 V (p. 2).
- Updated EMC standards.
- Deleted minimum magnetic field immunity specifications (not 100% tested).
- Updated thermal specifications (p. 7).

ISB-DS-001-IL260/1/2-V

Change
- VDE certification and UL approval for V-Series versions (6 kV reinforced isolation).

ISB-DS-001-IL260/1/2-U

Changes
- Updated VDE certification standard to VDE V 0884-10.
- Upgraded "VE" Version Surge Immunity specification to 12.8 kV.
- Upgraded "VE" Version VDE 0884-10 rating to reinforced insulation.
- Corrected QSOP pin width dimension (p. 10).

ISB-DS-001-IL260/1/2-T

Changes
- Increased V-Series isolation voltage to 6 kVrms.
- Increased typ. Total Barrier Thickness specification to 0.016 mm.
- Increased CTI min. specification to ≥600 V_{RMS}.

ISB-DS-001-IL260/1/2-S

Changes
- Added V-Series 5 kV isolation voltage versions.
- More detailed "Available Parts" table.

ISB-DS-001-IL260/1/2-R

Changes
- Added QSOP packages (-1 suffix).
- Revised and added details to thermal characteristic specifications (p. 2).
- Added VDE 0884 Safety-Limiting Values (p. 3).
- Added "Thermal Management" paragraph in Applications section.

ISB-DS-001-IL260/1/2-Q

Change
- IEC 60747-5-5 (VDE 0884) certification.

ISB-DS-001-IL260/1/2-P

Changes
- Tighter quiescent current specifications.
- Upgraded from MSL 2 to MSL 1.

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